Intel® Xeon® Processor E7 v4 Product Family

Datasheet Volume 2: Registers

May 2016

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Revision Number	Description	Date
001	• Initial release of the document.	May 2016

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1 Registers Overview and Configuration Process

The Intel® Xeon® processor E7 v4 product family contains one or more PCI devices within each individual functional block. The configuration registers for these devices are mapped as devices residing on the PCI Bus assigned for the processor socket.

Some features are only supported on specific SKUs. In such case the respective registers would only apply to the specific SKU which contains the feature support.

Refer to the *Intel® Xeon® Processor E5/E7 v4 Product Families Uncore Performance Monitoring Reference Manual* for details on Performance Monitoring Registers.

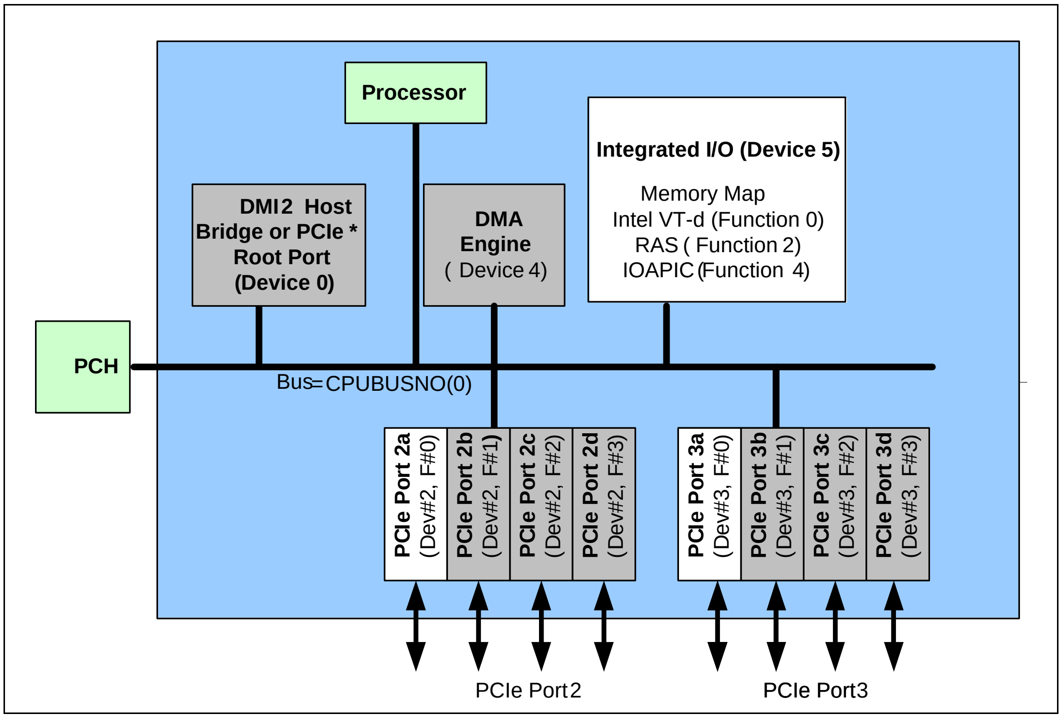
1.1 Platform Configuration Structure

The DMI2 physically connects the processor and the PCH. From a configuration standpoint the DMI2 is a logical extension of PCI Bus 0. DMI2 and the internal devices in the processor IIO and PCH logically constitute PCI Bus 0 to configuration software. As a result, all devices internal to the processor and the PCH appear to be on PCI Bus 0.

1.1.1 Processor IIO Devices (CPUBUSNO (0))

The processor IIO contains PCI devices within a single, physical component. The configuration registers for the devices are mapped as devices residing on PCI Bus “CPUBUSNO(0)” where CPUBUSNO(0) is programmable by BIOS.

Figure 1-1. Processor Integrated I/O Device Map

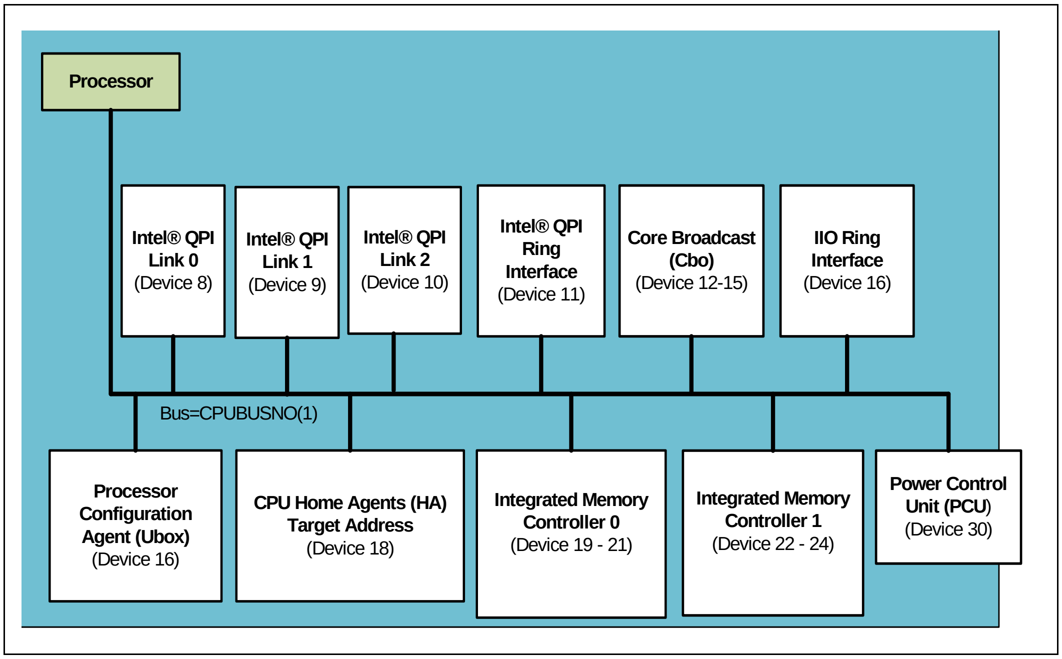


- **Device 0:** DMI2 Root Port. Logically this appears as a PCI device residing on PCI Bus 0. Device 0 contains the standard PCI header registers, extended PCI configuration registers and DMI2 device specific configuration registers.
- **Device 2:** PCI Express* Root Port 2a, 2b, 2c and 2d. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI Bus 0 and is compliant with *PCI Express Local Bus Specification Revision 2.0*. Device 2 contains the standard PCI Express/ PCI configuration registers including PCI Express Memory Address Mapping registers. It also contains the extended PCI Express configuration space that include PCI Express Link status/control registers and Virtual Channel controls.
- **Device 3:** PCI Express Root Port 3a, 3b, 3c and 3d. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI Bus 0 and is compliant with *PCI Express Local Bus Specification Revision 2.0*. Device 3 contains the standard PCI Express/ PCI configuration registers including PCI Express Memory Address Mapping registers. It also contains the extended PCI Express configuration space that include PCI Express error status/control registers and Virtual Channel controls.
- **Device 4:** Intel® QuickData Technology DMA. This device contains the Standard PCI registers for each of its functions. This device implements 8 functions for the 8 DMA Channels and also contains Memory Map I/O registers.
- **Device 5:** Integrated I/O Core. This device contains the Standard PCI registers for each of its functions. This device implements three functions; Function 0 contains Address Mapping, Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) related registers and other system management registers. Function 1 contains PCIe* and Memory Hot-Plug registers. Function 2 contains I/O RAS registers, Function 4 contains System Control/Status registers and miscellaneous control/status registers on power management and throttling.

1.1.2 Processor Uncore Devices (CPUBUSNO (1))

The configuration registers for these devices are mapped as devices residing on the PCI bus assigned for the processor socket. Bus number is derived by the max bus range setting and processor socket number.

Figure 1-2. Processor Uncore Devices Map



- **Device 8:** Intel® QuickPath Interconnect (Intel® QPI) Link 0. Device 8 contains the Intel QPI Link 0 registers.
- **Device 9:** Intel QPI Link 1. Device 9 contains the Intel QPI Link 1 registers.
- **Device 10:** Intel QPI Link 2. Device 10, Functions 0, 2, 3 contain the configurable Intel QPI Link 2 registers.
- **Device 11:** Intel QPI Ring Interface Device. Device 11 contains the processor Ring to Intel QPI registers.
- **Device 12 - 14:** Processor Caching Agent. Device 12 - 14 contain the Cbo Unicast configuration registers.
  — Implemented devices and functions in these devices vary based on SKU.
- **Device 15:** Processor Caching Agent. Device 15 contain the Cbo Broadcast configuration registers.
- **Device 16:** Integrated IO Ring Interface Device. Device 16, Functions 0, 1 contain the processor ring to PCI Express agent registers
- **Device 16:** Processor Configuration Agent. Device 16 contains the Processor Interrupt Event Handling (Ubox) registers.
- **Device 18:** Processor Home Agent(s) (HA). Functions 0-1 contain Home Agent 0 registers. Functions 4-5 contain Home Agent 1 registers. There is one Home Agent per Memory Controller.
- **Device 19 - 21:** Integrated Memory Controller 0 configuration registers. For SKUs with one IMC, this IMC supports up to 4 channels (0-3) off of IMC 0. This IMC supports 2 channels (0,1) and device 19 Functions 4, 5 (channel 2,3).

- **Device 22 - 23:** Integrated Memory Controller 1 configuration registers. This IMC supports 2 channels (2,3).
- **Device 30:** Processor Power Control Unit. Device 30 contain the PCU registers.

1.2 Configuration Register Rules

The Intel® Xeon® processor E7 v4 product family supports the following configuration register types:

- PCI Configuration Registers (CSRs): CSRs are chipset specific registers that are located at PCI defined address space.
- Machine Specific Registers (MSRs): MSRs are machine specific registers that can be accessed by specific read and write instructions. MSRs are OS ring 0 and BIOS accessible, though some can only be accessed in certain modes (that is, SMM mode).
- Memory-mapped I/O registers: These registers are mapped into the system memory map as MMIO low or MMIO high. They are accessed by any code typically an OS driver running on the platform. This register space is introduced with the integration of some of the chipset functionality.

1.2.1 CSR Access

Configuration space registers are accessed via the well known configuration transaction mechanism defined in the PCI specification and this uses the bus:device:function number concept to address a specific device's configuration space. If initiated by a remote CPU, accesses to PCI configuration registers are achieved via NcCfgRd/Wr transactions on Intel QPI.

All configuration register accesses are accessed over Message Channel through the Ubox but might come from a variety of different sources:

- Local cores
- Remote cores (over Intel QuickPath Interconnect)

Configuration registers can be read or written in Byte, WORD (16-bit), or DWORD (32-bit) quantities. *Accesses larger than a DWORD to PCI Express configuration space results in unexpected behavior.* All multi-byte numeric fields use "little-endian" ordering (that is, lower addresses contain the least significant parts of the field).

1.2.1.1 PCI Bus Number

In the tables shown for IIO devices (0 - 7), the PCI Bus numbers are all marked as "Bus 0". This means that the actual bus number is variable depending on which socket is used. The specific bus number for all PCIe devices in the Intel® Xeon® Processor E7 v4 product family is specified in the CPUBUSNO register which exists in the I/O module's configuration space. Bus number is derived by the max bus range setting and processor socket number.

1.2.1.2 Uncore Bus Number

In the tables shown for Uncore devices (8 - 31), the PCI Bus numbers are all marked as "bus 1". This means that the actual bus number is CPUBUSNO(1) where CPUBUSNO(1) is programmable by BIOS depending on which socket is used. The specific bus number for all PCIe devices in the Intel® Xeon® Processor E7 v4 product family is specified in the CPUBUSNO register.

1.2.1.3 Device Mapping

Each component in the processor is uniquely identified by a PCI bus address consisting of Bus Number, Device Number and Function Number. Device configuration is based on the PCI Type 0 configuration conventions. All processor registers appear on the PCI bus assigned for the processor socket. Bus number is derived by the max bus range setting and processor socket number.

Table 1-1. Functions Specifically Handled by the Processor (Sheet 1 of 2)

Register Group	DID	Device	Function	Comment
DMI2	2F00h	0	0	x4 link from Processor to PCH
PCI Express Root Port in DMI2 Mode	2F01h	0	0	Device 0 operating as a x4 PCI Express Port instead of a link to the PCH
PCI Express Root Port 2	2F04h, 2F05h, 2F06h, 2F07h	2	0-3	PCIe Device 2 Root Ports x16, x8 or x4 max link width
PCI Express Root Port 3	2F08, 2F09h, 2FOAh, 2F0Bh	3	0-3	PCIe Device 3 Root Ports x16, x8 or x4 max link width
IIO	2F28h	5	0	Address Map, Intel VT-d, System Management
IIO	2F29h	5	1	Hot-Plug
IIO	2F2Ah	5	2	RAS, Control Status and Global Errors
IIO	2F2Ch	5	4	I/O APIC
Intel QuickData Technology	2F20h, 2F21h, 2F22h, 2F23h, 2F24h, 2F25h, 2F26h, 2F27h	4	0-7	DMA Channel 0 to Channel 7
Intel QPI Link	2F80h	8	0	Intel QPI Link 0
Intel QPI Link	2F90h	9	0	Intel QPI Link 1
Intel QPI Link	2F40h	10	0	Intel QPI Link 2
PCU	2F98h, 2F99h, 2F9Ah 2FC0h 2F9Ch	30	0-4	Power Control Unit
UBOX	2F1Eh	16	5	Scratchpad and Semaphores
UBOX	2F7Dh	16	6	Scratchpad and Semaphores
UBOX	2F1F	16	7	Scratchpad and Semaphores
Integrated Memory Controller 0	2FA8h, 2F71	19	0,1	IMC Main
Integrated Memory Controller 0	2FAAh, 2FABh, 2FACh, 2FADh	19	2-5	IMC Channel 0-3 Target Address Decoder Registers
Integrated Memory Controller 0	2FB4, 2FB5, 2FB0, 2FB1	20,21	0,1	IMC Channel 0-3 Registers

Table 1-1. Functions Specifically Handled by the Processor (Sheet 2 of 2)

Register Group	DID	Device	Function	Comment
Integrated Memory Controller 0	2FB6, 2FB7, 2FB2, 2FB3	20,21	2,3	IMC Channel 0-3 Registers
Integrated Memory Controller 1	2F68h, 2F79h,	22	0,1	IMC Main
Integrated Memory Controller 1	2F6A, 2F6B, 2F6Ch, 2F6Dh	22	2-5	IMC Channel 0-3 Target Address Decoder Registers
Integrated Memory Controller 1	2FD4, 2FD5, 2FD0, 2FD1	23,24	0,1	IMC Channel 0-3 Registers
Integrated Memory Controller 1	2FD6, 2FD7, 2FD2, 2FD3	23,24	2,3	IMC Channel 0-3 Registers
R2PCIe	2F1Dh	16	0	Integrated IO Ring Interface
R2PCIe	2F34h	16	1	PCI Express Ring Performance Monitoring
R3QPI	2F81h, 2F41,	11	0,4	Intel QPI Ring Interface
R3QPI	2F36h, 2F37h	11	1,2	Intel QPI Ring Performance Monitoring

1.2.1.4 Unimplemented Devices/Functions and Registers

Configuration reads to unimplemented functions and devices will return all ones emulating a master abort response. Note that there is no asynchronous error reporting that happens when a configuration read master aborts. Configuration writes to unimplemented functions and devices will return a normal response.

Software should not attempt or rely on reads or writes to unimplemented registers or register bits. Unimplemented registers should return all zeros when read. Writes to unimplemented registers are ignored. For configuration writes to these register (require a completion), the completion is returned with a normal completion status (not master-aborted).

1.2.1.5 Device Hiding

The Intel® Xeon® processor E7 v4 product family provides a mechanism by which various PCI devices or functions within the unit can be hidden from the host configuration software; that is, all PCI configuration accesses to the devices' configuration space from Intel QPI will be master aborted. This mechanism is needed in cases where a device or function is not used or is available for use, because either the device is turned off or the device is not serving any meaningful purpose in a given platform configuration. This hiding mechanism is implemented via the DEVHIDE register.

1.2.2 MSR Access

Machine specific registers are architectural and only accessed by using specific ReadMSR/WriteMSR instructions. MSRs are always accessed as a naturally aligned 4 or 8 byte quantity.

For common IA-32 architectural MSRs, please refer to the *Intel® 64 and IA-32 Software Developer's Manual*.

1.2.3 Memory-Mapped I/O Registers

The PCI standard provides not only configuration space registers but also registers which reside in memory-mapped space. For PCI devices, this is typically where the majority of the driver programming occurs and the specific register definitions and characteristics are provided by the device manufacturer. Access to these registers are typically accomplished via CPU reads and writes to non-coherent (UC) or write-combining (WC) space.

Reads and writes to memory-mapped registers can be accomplished with 1, 2, 4 or 8 byte transactions.

1.3 Register Terminology

The bits in configuration register descriptions will have an assigned attribute from the following table. Bits without a Sticky attribute are set to their default value by a hard reset.

Table 1-2. Register Attributes Definitions (Sheet 1 of 2)

Attr	Description
RO	**Read Only:** These bits can only be read by software, writes have no effect. The value of the bits is determined by the hardware only.
RW	**Read / Write:** These bits can be read and written by software.
RC	**Read Clear Variant:** These bits can be read by software, and the act of reading them automatically clears them. HW is responsible for writing these bits, and therefore the -V modifier is implied.
W1S	**Write 1 to Set:** Writing a 1 to these bits will set them to 1. Writing 0 will have no effect. Reading will return indeterminate values and read ports are not requited on the register.
WO	**Write Only:** These bits can only be written, reads return indeterminate values.
RW-O	**Read / Write Once:** These bits can be read by software. After reset, these bits can only be written by software once, after which the bits becomes 'Read Only'.
RW-L	**Read / Write Lock:** These bits can be read and written by software. Hardware can make these bits 'Read Only' via a separate configuration bit or other logic.
RW1C	**Read / Write 1 to Clear:** These bits can be read and cleared by software. Writing a '1' to a bit clears it, while writing a '0' to a bit has no effect.
ROS	**RO Sticky:** These bits can only be read by software, writes have no effect. The value of the bits is determined by the hardware only. These bits are only re-initialized to their default value by a PWRGOOD reset.
RW1S	**Read, Write 1 to Set:** These bits can be read. Writing a 1 to a given bit will set it to 1. Writing a 0 to a given bit will have no effect. It is not possible for software to set a bit to "0". The 1->0 transition can only be performed by hardware. These registers are implicitly -V.
RWS	**R / W Sticky:** These bits can be read and written by software. These bits are only re-initialized to their default value by a PWRGOOD reset.
RW1CS	**R / W1C Sticky:** These bits can be read and cleared by software. Writing a '1' to a bit clears it, while writing a '0' to a bit has no effect. These bits are only re-initialized to their default value by a PWRGOOD reset.

Table 1-2. Register Attributes Definitions (Sheet 2 of 2)

Attr	Description
RW-LB	**Read / Write Lock Bypass**: Similar to RWL, these bits can be read and written by software. HW can make these bits "Read Only" via a separate configuration bit or other logic. However, RW-LB is a special case where the locking is controlled by the lock-bypass capability that is controlled by the lock-bypass enable bits. Each lock-bypass enable bit enables a set of config request sources that can bypass the lock. The requests sourced from the corresponding bypass enable bits will be lock-bypassed (i.e. RW).
RO-FW	**Read Only Forced Write:** These bits are read only from the perspective of the cores.
RWS-O	**R / W Sticky Once:** If a register is both sticky and "once" then the sticky value applies to both the register value and the "once" characteristic. Only a PWRGOOD reset will reset both the value and the "once" so that the register can be written to again.
RW-V	**R / W Volatile:** These bits may be modified by hardware. Typically, this occurs based on values from hardware configuration straps for functions such as DMI2 and PCIe I/O configuration. They also could be changed based on status or modes within internal state machines. Software cannot expect the values to stay unchanged.
RWS-L	**R / W Sticky Locked:** If a register is both sticky and locked, then the sticky behavior only applies to the value. The sticky behavior of the lock is determined by the register that controls the lock.
RV, RSVD	**Reserved:** These bits are reserved for future expansion and their value must not be modified by software. When writing these bits, software must preserve the value read.

1.4 Protected Processor Inventory Number

Protected Processor Inventory Number (PPIN) is a solution for inventory management available on Intel Xeon processor E7 v4 product family for use in server platforms.

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2 Integrated Memory Controller (iMC) Configuration Registers

The Integrated Memory Controller registers are listed below and are specific to the Intel® Xeon® processor E7 v4 product family.

2.1 Device 19,22 Function 0

	100h	SMB_STAT_0	180h
MH_MAINCNTL	104h	SMBCMD_0	184h
	108h	SMBCntl_0	188h
MH_SENSE_500NS_CFG	10Ch	SMB_TSOD_POLL_RATE_CNTR_0	18Ch
MH_DTYCYC_MIN_ASRT_CNTR_0	110h	SMB_STAT_1	190h
MH_DTYCYC_MIN_ASRT_CNTR_1	114h	SMBCMD_1	194h
MH_IO_500NS_CNTR	118h	SMBCntl_1	198h
MH_CHN_ASTN	11Ch	SMB_TSOD_POLL_RATE_CNTR_1	19Ch
	120h	SMB_PERIOD_CFG	1A0h
MH_EXT_STAT	124h	SMB_PERIOD_CNTR	1A4h
	128h	SMB_TSOD_POLL_RATE	1A8h
	12Ch		1ACh
	130h		1B0h
	134h		1B4h
	138h		1B8h
	13Ch		1BCh
	140h		1C0h
	144h		1C4h
	148h		1C8h
	14Ch		1CCh
	150h		1D0h
	154h		1D4h
	158h		1D8h
	15Ch		1DCh
	160h		1E0h
	164h		1E4h
	168h		1E8h
	16Ch		1ECh
	170h		1F0h
	174h		1F4h
	178h		1F8h
	17Ch		1FCh

2.1.1 pxpcap

PCI Express Capability.

Type: CFG	PortID: N/A		
Bus: 1	Device: 19,22	Function: 0	
Offset: 0x40			

Bit	Attr	Default	Description
29:25	RO	0x0	Interrupt Message Number (interrupt_message_number): N/A for this device
24:24	RO	0x0	Slot Implemented (slot_implemented): N/A for integrated endpoints
23:20	RO	0x9	Device/Port Type (device_port_type): Device type is Root Complex Integrated Endpoint
19:16	RO	0x1	Capability Version (capability_version): PCI Express Capability is Compliant with Version 1.0 of the PCI Express Spec. Note: This capability structure is not compliant with Versions beyond 1.0, since they require additional capability registers to be reserved. The only purpose for this capability structure is to make enhanced configuration space available. Minimizing the size of this structure is accomplished by reporting version 1.0 compliance and reporting that this is an integrated root port device. As such, only three Dwords of configuration space are required for this structure.
15:8	RO	0x0	Next Capability Pointer (next_ptr): Pointer to the next capability. Set to 0 to indicate there are no more capability structures.
7:0	RO	0x10	Capability ID (capability_id): Provides the PCI Express capability ID assigned by PCI-SIG.

2.1.2 mcmtr

Memory Technology

Type: CFG Bus: 1 Offset: 0x7c	PortID: N/A Device: 19,22	Function: 0	
Bit	**Attr**	**Default**	**Description**
21:18	RW_LB	0x0	CHN_DISABLE(chn_disable): Channel disable control. When set, the corresponding channel is disabled.
17:16	RW_LB	0x0	pass76(pass76): 00: do not alter ChnAdd calculation 01: replace ChnAdd[6] with SysAdd[6] 10: Reserved 11: replace ChnAdd[7:6] with SysAdd[7:6]
14	RW_LB	0x0	ddr4 (ddr4): DDR4 mode
13:12	RW_LB	0x0	IMC_MODE (imc_mode): Memory mode: 00: Native DDR 10: Intel® Scalable Memory Interconnect (Intel® SMI) 2 1:1 Subchannel Lockstep Mode 11: Intel SMI 2 2:1 Performance Mode All others reserved.
9:9	RW_LB	0x0	BANK_XOR_ENABLE (bank_xor_enable): When set, this bit will enable bank XOR'ing. This is targeted at workloads that bank thrashing caused by certain stride or page mappings. 0: TBank selection is done using rank address bits 12:17:18 for open page mapping and bits 6:7:8 for close page mapping. 1: Bank XOR'ing enabled. Bank selection is done using rank address bits: • (12^19):(17^20):(18^21) for open page mapping • (6^19):(7^20):(8^21) for close page mapping
8:8	RW_LB	0x0	NORMAL (normal): 0: Training mode 1: Normal Mode
3:3	RW_LBV	0x0	DIR_EN (dir_en): If the directory disabled in SKU, this register bit is set to Read-Only (RO) with 0 value, that is, directory is disabled. When this bit is set to zero, IMC ECC code will use the non-directory CRC-16. If the SKU supports directory and enabled, i.e. directory is not disabled, the DIR_EN bit can be set by BIOS, MC ECC will use CRC-15 in the first 32B code word to yield one directory bit. It is important to know that changing this bit will require BIOS to re-initialize the memory.
2:2	RW_LBV	0x0	ECC_EN (ecc_en): ECC enable. DISECC will force override this bit to 0.
1:1	RW_LBV	0x0	LS_EN (ls_en): Use lock-step channel mode if set; otherwise, independent channel mode. This field should only be set for native DDR lockstep.
0:0	RW_LB	0x0	CLOSE_PG (close_pg): Use close page address mapping if set; otherwise, open page.

2.1.3 tadwayness_[0:11]

TAD Range Wayness, Limit and Target.

There are total of 12 TAD ranges (N + P + 1 = number of TAD ranges; P = how many times channel interleave changes within the SAD ranges.).

Note for mirroring configuration:

For 1-way interleave, channel 0-2 mirror pair: target list <0,2,x,x>, TAD ways = “00”

For 1-way interleave, channel 1-3 mirror pair: target list <1,3,x,x>, TAD ways = “00”

For 2-way interleave, 0-2 mirror pair and 1-3 mirror pair: target list <0,1,2,3>, TAD ways = “01”

For 1-way interleave, lockstep mirroring, target list <0,2,x,x>, TAD ways = “00”

Type: CFG **PortID:** N/A
Bus: 1 **Device:** 19,22 **Function:** 0
Offset: 0x80, 0x84, 0x88, 0x8c, 0x90, 0x94, 0x98, 0x9c, 0xa0, 0xa4, 0xa8, 0xac

Bit	Attr	Default	Description
31:12	RW_LB	0x0	TAD_LIMIT (tad_limit): Highest address of the range in system address space, 64MB granularity, i.e. TADRANGLIMIT[45:26].
11:10	RW_LB	0x0	TAD_SKT_WAY (tad_skt_way): socket interleave wayness 00 = 1 way, 01 = 2 way, 10 = 4 way, 11 = 8 way.
9:8	RW_LB	0x0	TAD_CH_WAY (tad_ch_way): channel interleave wayness 00 - interleave across 1 channel or mirror pair 01 - interleave across 2 channels or mirror pairs 10 - interleave across 3 channels 11 - interleave across 4 channels This parameter effectively tells iMC how much to divide the system address by when adjusting for the channel interleave. Since both channels in a pair store every line of data, divide by 1 when interleaving across one pair and 2 when interleaving across two pairs. For HA, it tells how may channels to distribute the read requests across. When interleaving across 1 pair, this distributes the reads to two channels, when interleaving across 2 pairs, this distributes the reads across 4 pairs. Writes always go to both channels in the pair when the read target is either channel.
7:6	RW_LB	0x0	TAD_CH_TGT3 (tad_ch_tgt3): target channel for channel interleave 3 (used for 4-way TAD interleaving). This register is used in the iMC only for reverse address translation for logging sparepatrol errors, converting a rank address back to a system address.
5:4	RW_LB	0x0	TAD_CH_TGT2 (tad_ch_tgt2): target channel for channel interleave 2 (used for 3/4-way TAD interleaving).
3:2	RW_LB	0x0	TAD_CH_TGT1 (tad_ch_tgt1): target channel for channel interleave 1 (used for 2/3/4-way TAD interleaving).
1:0	RW_LB	0x0	TAD_CH_TGT0 (tad_ch_tgt0): target channel for channel interleave 0 (used for 1/2/3/4-way TAD interleaving).

2.1.4 mc_init_state_g

Initialization state for boot and training.

Type: CFG Bus: 1 Offset: 0xb4		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
14:14	RWS_L	0x0	reset_io_vmse_rhs: Training Reset for DDRIO.
13:13	RWS_L	0x0	reset_vmse2to1 — Reset is used to set up Intel SMI 2 2:1 mode correctly in DDRIO. The register must be set and reset after the IMC mode register is configured to Intel SMI 2 2:1 mode.
12:9	RWS_L	0x0	cs_oe_en:
8:8	RWS_L	0x1	MC is in SR (safe_sr): This bit indicates if it is safe to keep the MC in self refresh (SR) during MC-reset. If it is clear when reset occurs, it means that the reset is without warning and the DDR-reset should be asserted. If set when reset occurs, it indicates that DDR is already in SR and it can keep it this way. This bit can also indicate MRC if reset without warning has occurred, and if it has, cold-reset flow should be selected. BIOS need to clear this bit at MRC entry.
7:7	RW_L	0x0	MRC_DONE (mrc_done): This bit indicates the PCU that the MRC is done, IMC is in normal mode, ready to serve. MRC should set this bit when MRC is done, but it doesn't need to wait until training results are saved in BIOS flash.
5:5	RW_L	0x1	DDRIO Reset (reset_io): Training Reset for DDRIO. Make sure this bit is cleared before enabling DDRIO.
3:3	RW_L	0x0	Refresh Enable (refresh_enable): If cold reset, this bit should be set by BIOS after: 1) Initializing the refresh timing parameters 2) Running DDR through reset ad init sequence. If warm reset or S3 exit, this bit should be set immediately after SR exit.
2:2	RW_L	0x0	DCLK Enable (for all channels) (dclk_enable):
1:1	RW_L	0x1	DDR_RESET (ddr_reset): DIMM reset. Controls all channels.

2.1.5 rcomp_timer

RCOMP wait timer. Defines the time from IO starting to run RCOMP evaluation until RCOMP results are definitely ready. This counter is added in order to keep determinism of the process if operated in different mode. This register also indicates that first RCOMP has been done.

Type: CFG Bus: 1 Offset: 0xc0		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW_V	0x0	rcomp_in_progress: RCOMP in progress status bit

Type: CFG Bus: 1 Offset: 0xc0		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
30:30	RW	0x0	rcomp: RCOMP start via message channel control for BIOS. RCOMP start only triggered when the register bit output is changing from 0 -> 1. iMC is not be responsible for clearing this bit. When Rcomp is done via first_rcomp_done bit field.
21:21	RW	0x0	ignore_mdll_locked_bit Ignore DDRIO MDLL lock status during rcomp when set.
20:20	RW	0x0	no_mdll_fsm_override: Do not force DDRIO MDLL on during rcomp when set.
16:16	RW_LV	0x0	First RCOMP has been done in DDRIO (first_rcomp_done): This is a status bit that indicates the first RCOMP has been completed. It is cleared on reset, and set by IMC HW when the first RCOMP is completed. BIOS should wait until this bit is set before executing any DDR command.
15:0	RW	0xc00	COUNT (count): DCLK cycle count that IMC needs to wait from the point it has triggered RCOMP evaluation until it can trigger the load to registers.

2.1.6 mh_sense_500ns_cfg

MEMHOT Sense and 500 ns Config.

Type: CFG Bus: 1 Offset: 0x10c		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
25:16	RW	0xc8	MH_SENSE_PERIOD (mh_sense_period): MEMHOT Input Sense Period in number of CNTR_500_NANOSEC. BIOS calculate number of CNTR_500_NANOSEC for 50 micro-sec / 100 micro-sec / 200 micro-sec / 400 micro-sec.
15:13	RW	0x2	MH_IN_SENSE_ASSERT (mh_in_sense_assert): MEMHOT Input Sense Assertion Time in number of CNTR_500_NANOSEC. BIOS calculate number of CNFG_500_NANOSEC for 1 micro-sec / 2 micro-sec inputsense duration. MH_IN_SENSE_ASSERT ranges: 0 or 1: Reserved 2 - 7: 1 micro-sec - 3.5 micro-sec sense assertion time in 500nsec increment.
9:0	RW-LS	0x190	CNFG_500_NANOSEC (cnfg_500_nanosec): 500ns equivalent in DCLK. BIOS calculate number of DCLK to be equivalent to 500 nanoseconds. This value is loaded into CNTR_500_NANOSEC when it is decremented to zero.

2.1.7 mh_dtycyc_min_asrt_cntr_[0:1]

MEMHOT Duty Cycle Period and Min Assertion Counter.

Type: CFG	PortID: N/A		
Bus: 1	Device: 19,22	Function: 0	
Offset: 0x110, 0x114			

Bit	Attr	Default	Description
31:20	RO_V	0x0	MH_MIN_ASRTN_CNTR (mh_min_asrtn_cntr): MEM_HOT[1:0]# Minimum Assertion Time Current Count in number of CNTR_500_NANOSEC decrement by 1 every CNTR_500_NANOSEC. When the counter is zero, the counter is remain at zero and it is only loaded with MH_MIN_ASRTN only when MH_DUTY_CYC_PRD_CNTR is reloaded.
19:0	RW_LV	0x0	MH_DUTY_CYC_PRD_CNTR (mh_duty_cyc_prd_cntr): MEM_HOT[1:0]# DUTY Cycle Period Current Count in number of CNTR_500_NANOSEC decrement by 1 every CNTR_500_NANOSEC. When the counter is zero, the next cycle is loaded with MH_DUTY_CYC_PRD.

2.1.8 mh_io_500ns_cntr

MEMHOT Input Output and 500 ns Counter.

Type: CFG Bus: 1 Offset: 0x118		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
31:22	RW_LV	0x0	MH1_IO_CNTR (mh1_io_cntr): MEM_HOT[1:0]# Input Output Counter in number of CNTR_500_NANOSEC. When MH0_IO_CNTR is zero, the counter is loaded with MH_SENSE_PERIOD in the next CNTR_500_NANOSEC. When count is greater than MH_IN_SENSE_ASSERT, the MEM_HOT1# output driver may be turn on if the corresponding MEM_HOT#event is asserted. The receiver is turned off during this time. When count is equal or less than MH_IN_SENSE_ASSERT, MEM_HOT[1:0]# output is disabled and receiver is turned on. Hardware will decrement this counter by 1 every time CNTR_500_NANOSEC is decremented to zero. When the counter is zero, the next CNFG_500_NANOSEC count is loaded with MH_IN_SENSE_ASSERT.
21:12	RW_LV	0x0	MH0_IO_CNTR (mh0_io_cntr): MEM_HOT[1:0]# Input Output Counter in number of CNTR_500_NANOSEC. When MH_IO_CNTR is zero, the counter is loaded with MH_SENSE_PERIOD in the next CNTR_500_NANOSEC. When count is greater than MH_IN_SENSE_ASSERT, the MEM_HOT[1:0]# output driver may be turn on if the corresponding MEM_HOT#event is asserted. The receiver is turned off during this time. When count is equal or less than MH_IN_SENSE_ASSERT, MEM_HOT[1:0]# output is disabled and receiver is turned on. BIOS calculate number of CNTR_500_NANOSEC hardware will decrement this register by 1 every CNTR_500_NANOSEC. When the counter is zero, the next CNTR_500_NANOSEC count is loaded with MH_IN_SENSE_ASSERT.
9:0	RW_LV	0x0	CNTR_500_NANOSEC (cntr_500_nanosec): 500 ns base counters used for the MEMHOT counters and the SMBus counters. BIOS calculate number of DCLK to be equivalent to 500 nanoseconds. CNTR_500_NANOSEC hardware will decrement this register by 1 every CNTR_500_NANOSEC. When the counter is zero, the next CNTR_500_NANOSEC count is loaded with CNFG_500_NANOSEC.

2.1.9 mh_chn_astn

MEMHOT Domain Channel Association.

Type: CFG Bus: 1 Offset: 0x11c		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
23:20	RO	0xb	MH1_2ND_CHN_ASTN (mh1_2nd_chn_astn): MemHot[1]# 2nd Channel Association bit 23: is valid bit. Note: Valid bit means the association is valid and it does not implies the channel is populated. bit 22-20: 2nd channel ID within this MEMHOT domain.
19:16	RO	0xa	MH1_1ST_CHN_ASTN (mh1_1st_chn_astn): MemHot[1]# 1st Channel Association bit 19: is valid bit. Note: Valid bit means the association is valid and it does not implies the channel is populated. bit 18-16: 1st channel ID within this MEMHOT domain.
7:4	RO	0x9	MH0_2ND_CHN_ASTN (mh0_2nd_chn_astn): MemHot[0]# 2nd Channel Association bit 7: is valid bit. Note: Valid bit means the association is valid and it does not implies the channel is populated. bit 6-4: 2nd channel ID within this MEMHOT domain.

Type: CFG Bus: 1 Offset: 0x11c		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
3:0	RO	0x8	MH0_1ST_CHN_ASTN (mh0_1st_chn_astn): MemHot[0]# 1st Channel Association bit 3: is valid bit. Note: Valid bit means the association is valid and it does not implies the channel is populated or exist. bit 2-0: 1st channel ID within this MEMHOT domain.

2.1.10 mh_ext_stat

Capture externally asserted MEM_HOT[1:0]# assertion detection.

Type: CFG Bus: 1 Offset: 0x124		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
1:1	RW1C	0x0	MH_EXT_STAT_1 (mh_ext_stat_1): MEM_HOT[1]# assertion status at this sense period. Set if MEM_HOT[1]# is asserted externally for this sense period, this running status bit will automatically updated with the next sensed value in the next MEMHOT input sense phase.
0:0	RW1C	0x0	MH_EXT_STAT_0 (mh_ext_stat_0): MEM_HOT[0]# assertion status at this sense period. Set if MEM_HOT[0]# is asserted externally for this sense period, this running status bit will automatically updated with the next sensed value in the next MEMHOT input sense phase.

2.1.11 smb_stat_[0:1]

SMBus Status. This register provides the interface to the SMBus/I2C* SCL and SDA signals that is used to access the Serial Presence Detect EEPROM (SPD) or Thermal Sensor on DIMM (TSOD) that defines the technology, configuration, and speed of the DIMMs controlled by iMC.

Type: CFG Bus: 1 Offset: 0x180,		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RO_V	0x0	SMB_RDO (smb_rdo): Read Data Valid This bit is set by iMC when the Data field of this register receives read data from the SPD/TSOD after completion of an SMBus read command. It is cleared by iMC when a subsequent SMBus read command is issued.
30:30	RO_V	0x0	SMB_WOD (smb_wod): Write Operation Done This bit is set by iMC when a SMBus Write command has been completed on the SMBus. It is cleared by iMC when a subsequent SMBus Write command is issued.

Type: CFG Bus: 1 Offset: 0x180,		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
29:29	RO_V	0x0	SMB_SBE (smb_sbe): SMBus Error This bit is set by iMC if an SMBus transaction (including the TSOD polling or message channel initiated SMBus access) that does not complete successfully (non-Ack has been received from slave at expected Ack slot of the transfer). If a slave device is asserting clock stretching, IMC does not have logic to detect this condition to set the SBE bit directly; however, the SMBus master will detect the error at the corresponding transaction's expected ACK slot. Once SMBUS_SBE bit is set, iMC stops issuing hardware initiated TSOD polling SMBUS transactions until the SMB_SBE is cleared. iMC will not increment the SMB_STAT_x.TSOD_SA until the SMB_SBE is cleared. Manual SMBus command interface is not affected, that is, new command issue will clear the SMB_SBE like A0 silicon behavior.
28:28	ROS_V	0x0	SMB_BUSY (smb_busy): SMBus Busy state. This bit is set by iMC while an SMBus/I2C command (including TSOD command issued from IMC hardware) is executing. Any transaction that is completed normally or gracefully will clear this bit automatically. By setting the SMB_SOFT_RST will also clear this bit. This register bit is sticky across reset so any surprise reset during pending SMBus operation will sustain the bit assertion across surprised warm-reset. BIOS reset handler can read this bit before issuing any SMBus transaction to determine whether a slave device may need special care to force the slave to idle state (e.g. via clock override toggling SMB_CKOVRD and/or via induced time-out by asserting SMB_CKOVRD for 25-35 ms).
27:24	RO_V	0x7	Last Issued TSOD Slave Address (tsod_sa): This field captures the last issued TSOD slave address. Here is the slave address and the DDR CHN and DIMM slot mapping: Slave Address: 0 -- Channel: Even Chn; Slot #: 0 Slave Address: 1 -- Channel: Even Chn; Slot #: 1 Slave Address: 2 -- Channel: Even Chn; Slot #: 2 Slave Address: 3 -- Channel: Even Chn; Slot #: 3 (reserved) Slave Address: 4 -- Channel: Odd Chn; Slot #: 0 Slave Address: 5 -- Channel: Odd Chn; Slot #: 1 Slave Address: 6 -- Channel: Odd Chn; Slot #: 2 Slave Address: 7 -- Channel: Odd Chn; Slot #: 3 (reserved) A value of 8 in this register indicates to poll MXB temperature rather than a DIMM temperature, values above 0x8 are invalid. Since this field only captures the TSOD polling slave address. During SMB error handling, software should check the hung SMB_TSOD_POLL_EN state before disabling the SMB_TSOD_POLL_EN in order to qualify whether this field is valid.
15:0	RO_V	0x0	SMB_RDATA (smb_rdata): Read DataHolds data read from SMBus Read commands. Since TSOD/EEPROM are I2C* devices and the byte order is MSByte first in a word read, reading of I2C using word read should return SMB_RDATA[15:8] = I2C_MSB and SMB_RDATA[7:0] = I2C_LSB. If reading of I2C using byte read, the SMB_RDATA[15:8] = dont care; SMB_RDATA[7:0] = readbyte. If there is a SMB slave connected on the bus, reading of the SMBus slave using word read returns SMB_RDATA[15:8] = SMB_LSB and SMB_RDATA[7:0] = SMB_MSB. If the software is not sure whether the target is I2C or SMBus slave, please use byte access.

2.1.12 smbcmd_[0:1]

A write to this register initiates a DIMM EEPROM access through the SMBus/I2C.

Type: CFG Bus: 1 Offset: 0x184,	PortID: N/A Device: 19,22	Function: 0	
Bit	**Attr**	**Default**	**Description**
31:31	RW_V	0x0	SMB_CMD_TRIGGER (smb_cmd_trigger): CMD trigger: After setting this bit to 1, the SMBus master will issue the SMBus command using the other fields written in SMBCMD_[0:1] and SMBCntl_[0:1]. Note: the '-V' in the attribute implies the hardware will reset this bit when the SMBus command is being started.
30:30	RWS	0x0	SMB_PNTR_SEL (smb_pntr_sel): Pointer Selection: SMBus/I2C present pointer based access enable when set; otherwise, use random access protocol. Hardware based TSOD polling will also use this bit to enable the pointer word read. Important Note: CPU hardware based TSOD polling can be configured with pointer based access. If software manually issue SMBus transaction to other address, i.e. changing the pointer in the slave device, it is software's responsibility to restore the pointer in each TSOD before returning to hardware based TSOD polling while keeping the SMB_PNTR_SEL = 1.
29:29	RWS	0x0	SMB_WORD_ACCESS (smb_word_access): Word access: SMBus/I2C word 2B access when set; otherwise, it is a byte access.
28:28	RWS	0x0	SMB_WRT_PNTR (smb_wrt_pntr): Bit[28:27] = 00: SMBus Read Bit[28:27] = 01: SMBus Write Bit[28:27] = 10: illegal combination Bit[28:27] = 11: Write to pointer register SMBus/I2C pointer update (byte). bit 30, and 29 are ignored. Note: SMBCntl_[0:1] [26] will NOT disable WrtPntr update command.
27:27	RWS	0x0	SMB_WRT_CMD (smb_wrt_cmd): When '0', it's a read command When '1', it's a write command
26:24	RWS	0x0	SMB_SA (smb_sa): Slave Address: This field identifies the DIMM SPD/TSOD to be accessed.
23:16	RWS	0x0	SMB_BA (smb_ba): Bus Txn Address: This field identifies the bus transaction address to be accessed. ***Note:*** In WORD access, 23:16 specifies 2B access address. In Byte access, 23:16 specified 1B access address.
15:0	RWS	0x0	SMB_WDATA (smb_wdata): Write Data: Holds data to be written by SPDW commands. Since TSOD/EEPROM are I2C devices and the byte order is MSByte first in a word write, writing of I2C using word write should use SMB_WDATA[15:8] = I2C_MSB and SMB_WDATA[7:0] = I2C_LSB. If writing of I2C using byte write, the SMB_WDATA[15:8] = dont care; SMB_WDATA[7:0] = writebyte. If we have a SMB slave connected on the bus, writing of the SMBus slave using word write should use SMB_WDATA[15:8] = SMB_LSB and SMB_WDATA[7:0] = SMB_MSB. It is software responsibility to figure out the byte order of the slave access.

2.1.13 smbcntl_[0:1]

SMBus Control.

Type: CFG Bus: 1 Offset: 0x188,			PortID: N/A Device: 19,22 Function: 0
Bit	**Attr**	**Default**	**Description**
31:28	RWS	0xa	SMB_DTI (smb_dti): Device Type Identifier: This field specifies the device type identifier. Only devices with this device-type will respond to commands. '0011' specifies TSOD. '1010' specifies EEPROM's. '0110' specifies a write-protect operation for an EEPROM. Other identifiers can be specified to target non-EEPROM devices on the SMBus. ***Note:*** IMC based hardware TSOD polling uses hardcoded DTI. Changing this field has no effect on the hardware based TSOD polling.
27:27	RWS_V	0x1	SMB_CKOVRD (smb_ckovrd): Clock Override '0' Clock signal is driven low, overriding writing a '1' to CMD. '1' Clock signal is released high, allowing normal operation of CMD. Toggling this bit can be used to 'budge' the port out of a 'stuck' state. Software can write this bit to 0 and the SMB_SOFT_RST to 1 to force hung SMBus controller and the SMB slaves to idle state without using power good reset or warm reset. ***Note:*** Software need to set the SMB_CKOVRD back to 1 after 35ms in order to force slave devices to time-out in case there is any pending transaction. The corresponding SMB_STAT_x.SMB_SBE error status bit may be set if there was such pending transaction time-out (non-graceful termination). If the pending transaction was a write operation, the slave device content may be corrupted by this clock override operation. A subsequent SMB command will automatically cleared the SMB_SBE. iMC added SMBus time-out control timer in B0. When the time-out control timer expired, the SMBCKOVRD# will “de-assert”, i.e. return to 1 value and clear the SMBSBE0.
26:26	RW_LB	0x1	SMB_DIS_WRT (smb_dis_wrt): Disable SMBus Write Writing a '0' to this bit enables CMD to be set to 1; Writing a 1 to force CMD bit to be always 0, i.e. disabling SMBus write. This bit can only be written in SMMode. SMBus Read is not affected. I2C Write Pointer Update Command is not affected. Important Note to BIOS: Since BIOS is the source to update SMBCNTL_x register initially after reset, it is important to determine whether the SMBus can have write capability before writing any upper bits (bit24-31) via byte-enable config write (or writing any bit within this register via 32b config write) within the SMBCNTL register.

Type: CFG Bus: 1 Offset: 0x188,		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
10:10	RW	0x0	SMB_SOFT_RST (smb_soft_rst): SMBus software reset strobe to graceful terminate pending transaction after ACK and keep the SMB from issuing any transaction until this bit is cleared. If slave device is hung, software can write this bit to 1 and the SMB_CKOVRD to 0 (for more than 35ms)to force hung the SMB slaves to time-out and put it in idle state without using power good reset or warm reset. ***Note:*** Software need to set the SMB_CKOVRD back to 1 after 35ms in order to force slave devices to time-out in case there is any pending transaction. The corresponding SMB_STAT_x.SMB_SBE error status bit may be set if there was such pending transaction time-out (non-graceful termination). If the pending transaction was a write operation, the slave device content may be corrupted by this clock override operation. A subsequent SMB command will automatically cleared the SMB_SBE. If the IMC HW perform SMB time-out with the SMB_SBE_EN = 1. Software should simply clear the SMB_SBE and SMB_SOFT_RST sequentially after writing the SMB_CKOVRD = 0 and SMB_SOFT_RST = 1 asserting clock override and perform graceful txn termination. Hardware will automatically de-assert the SMB_CKOVRD update to 1 after the pre-configured 35ms/65ms time-out.
9:9	RW_LB	0x0	start_tsod_poll: This bit starts the reading of all enabled devices. Note that the hardware will reset this bit when the SMBus polling has started.
8:8	RW_LB	0x0	SMB_TSOD_POLL_EN (smb_tsod_poll_en): TSOD polling enable '0': disable TSOD polling and enable SPDCMD accesses. '1': disable SPDCMD access and enable TSOD polling. It is important to make sure no pending SMBus transaction and the TSOD polling must be disabled (and pending TSOD polling must be drained) before changing the TSOD_POLL_EN.
7:0	RW_LB	0x0	TSOD_PRESENT for the lower and upper channels (tsod_present): DIMM slot mask to indicate whether the DIMM is equipped with TSOD sensor. Bit 7: must be programmed to zero. Upper channel slot #3 is not supported Bit 6: TSOD PRESENT at upper channel (ch 1 or ch 3) slot #2 Bit 5: TSOD PRESENT at upper channel (ch 1 or ch 3) slot #1 Bit 4: TSOD PRESENT at upper channel (ch 1 or ch 3) slot #0 Bit 3: must be programmed to zero. Lower channel slot #3 is not supported Bit 2: TSOD PRESENT at lower channel (ch 0 or ch 2) slot #2 Bit 1: TSOD PRESENT at lower channel (ch 0 or ch 2) slot #1 Bit 0: TSOD PRESENT at lower channel (ch 0 or ch 2) slot #0

2.1.14 smb_tsod_poll_rate_cntr_[0:1]

Type: CFG Bus: 1 Offset: 0x18c,		PortID: N/A Device: 19,22	Function: 0
Bit	**Attr**	**Default**	**Description**
17:0	RW_LV	0x0	SMB_TSOD_POLL_RATE_CNTR (smb_tsod_poll_rate_cntr): TSOD poll rate counter. When it is decremented to zero, reset to zero or written to zero, SMB_TSOD_POLL_RATE value is loaded into this counter and appear the updated value in the next DCLK.

2.1.15 smb_period_cfg

SMBus Clock Period Config.

Type: CFG Bus: 1 Offset: 0x1a0	PortID: N/A Device: 19,22		Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RWS	0x445c	Reserved
15:0	RWS	0xfa0	SMB_CLK_PRD (smb_clk_prd): This field specifies both SMBus Clock in number of DCLK. Note: In order to generate a 50% duty cycle SCL, half of the SMB_CLK_PRD is used to generate SCL high. SCL must stay low for at least another half of the SMB_CLK_PRD before pulling high. It is recommend to program an even value in this field since the hardware is simply doing a right shift for the divided by 2 operation. Note the 100 KHz SMB_CLK_PRD default value is calculated based on 800 MTs (400 MHz) DCLK.

2.1.16 smb_period_cntr

SMBus Clock Period Counter.

Type: CFG Bus: 1 Offset: 0x1a4	PortID: N/A Device: 19,22		Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RO_V	0x0	SMB1_CLK_PRD_CNTR (smb1_clk_prd_cntr): SMBus #1 Clock Period Counter for Ch 23. This field is the current SMBus Clock Period Counter Value.
15:0	RO_V	0x0	SMB0_CLK_PRD_CNTR (smb0_clk_prd_cntr): SMBus #0 Clock Period Counter for Ch 01. This field is the current SMBus Clock Period Counter Value.

2.1.17 smb_tsod_poll_rate

Type: CFG Bus: 1 Offset: 0x1a8	PortID: N/A Device: 19,22		Function: 0
Bit	**Attr**	**Default**	**Description**
17:0	RWS	0x3e800	SMB_TSOD_POLL_RATE (smb_tsod_poll_rate): TSOD poll rate configuration between consecutive TSOD accesses to the TSOD devices on the same SMBus segment. This field specifies the TSOD poll rate in number of 500 ns per CNFG_500_NANOSEC register field definition.

2.2 Device 19,22 Function 1

DID		VID		0h	SPAREADDRESSLO	80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h	SPARECTL	90h
				14h	SSRSTATUS	94h
				18h	SCRUBADDRESSLO	98h
				1Ch	SCRUBADDRESSHI	9Ch
				20h	SCRUBCTL	A0h
				24h		A4h
				28h	SPAREINTERVAL	A8h
SDID		SVID		2Ch	RASENABLES	ACh
				30h		B0h
			CAPPTR	34h	SMISPARECTL	B4h
				38h	LEAKY_BUCKET_CFG	B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
PXPCAP				40h	LEAKY_BUCKET_CNTR_LO	C0h
				44h	LEAKY_BUCKET_CNTR_HI	C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h		D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
				68h		E8h
				6Ch		ECh
				70h		F0h
				74h		F4h
				78h		F8h
				7Ch		FCh

2.2.1 pxpcap

Type: CFG **PortID:** N/A
Bus: 1 **Device:** 19,22 **Function:** 1
Offset: 0x40

Bit	Attr	Default	Description
29:25	RO	0x0	Interrupt Message Number (interrupt_message_number): NA for this device

Type: CFG Bus: 1 Offset: 0x40		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
24:24	RO	0x0	Slot Implemented (slot_implemented): NA for integrated endpoints
23:20	RO	0x9	Device/Port Type (device_port_type): Device type is Root Complex Integrated Endpoint
19:16	RO	0x1	Capability Version (capability_version): PCI Express Capability is Compliant with Version 1.0 of the PCI Express Spec. ***Note:*** This capability structure is not compliant with Versions beyond 1.0, since they require additional capability registers to be reserved. The only purpose for this capability structure is to make enhanced configuration space available. Minimizing the size of this structure is accomplished by reporting version 1.0 compliancy and reporting that this is an integrated root port device. As such, only three Dwords of configuration space are required for this structure.
15:8	RO	0x0	Next Capability Pointer (next_ptr): Pointer to the next capability. Set to 0 to indicate there are no more capability structures.
7:0	RO	0x10	Capability ID (capability_id): Provides the PCI Express capability ID assigned by PCI-SIG.

2.2.2 spareaddresslo

Spare Address Low

Always points to the lower address for the next sparing operation. This register will not be affected by the HA access to the spare source rank during the HA window.

Type: CFG Bus: 1 Offset: 0x80		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
30:0	RW_LV	0x0	RANKADD (rankadd): Always points to the lower address for the next sparing operation. This register will not be affected by the HA access to the spare source rank during the HA window.

2.2.3 sparectl

Type: CFG Bus: 1 Offset: 0x90		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
29:29	RW_LB	0x0	DisWPQWM (diswpqwm): Disable WPQ level based water mark, so that sparing wm is only based on HaFifoWM. If DisWPQWM is clear, the spare window is started when the number of hits to the failed DIMM exceed max (# of credits in WPQ not yet returned to the HA, HaFifoWM). If DisWPQWM is set, the spare window starts when the number of hits to the failed DIMM exceed HaFifoWM. In either case, if the number of hits to the failed DIMM do not hit the WM, the spare window will still start after SPAREINTERVAL.NORMOPDUR timer expiration.
28:24	RW_LB	0x0	HaFifoWM (hafifowm): minimum water mark for HA writes to failed rank. Actual wm is max of WPQ credit level and HaFifoWM. When wm is hit the HA is backpressured and a sparing window is started. If DisWPQWM is clear, the spare window is started when the number of hits to the failed DIMM exceed max (# of credits in WPQ not yet returned to the HA, HaFifoWM). If DisWPQWM is set, the spare window starts when the number of hits to the failed DIMM exceed HaFifoWM.
23:16	RW	0x0	SCRATCH_PAD (scratch_pad): This field is available as a scratch pad.
10:8	RW_LB	0x0	DST_RANK (dst_rank): Destination logical rank used for the memory copy.
6:4	RW_LB	0x0	SRC_RANK (src_rank): Source logical rank that provides the data to be copied.
3:2	RW_LB	0x0	CHANNEL SELECT FOR THE SPARE COPY (chn_sel): Since there is only one spare-copy logic for all channels, this field selects the channel or channel-pair for the spare-copy operation. For independent channel operation: 00 = channel 0 is selected for the spare-copy operation 01 = channel 1 is selected for the spare-copy operation 10 = channel 2 is selected for the spare-copy operation 11 = channel 3 is selected for the spare-copy operation For lock-step channel operation: 0x = channel 0 and channel 1 are selected for the spare-copy operation 1x = channel 2 and channel 3 are selected for the spare-copy operation
0:0	RW_LBV	0x0	SPARE_ENABLE (spare_enable): Spare enable when set to 1. Hardware clear after the sparing completion.

2.2.4 ssrstatus

Provides the status of a spare-copy memory Init operation.

Type: CFG Bus: 1 Offset: 0x94		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
2:2	RW1C	0x0	PATCMPLT (patcmplt): All memory has been scrubbed. Hardware sets this bit each time the patrol engine steps through all memory locations. If software wants to monitor 0 ---> 1 transition after the bit has been set, the software will need to clear the bit by writing a one to clear this bit in order to distinguish the next patrol scrub completion. Clearing the bit will not affect the patrol scrub operation.
1:1	RO_V	0x0	SPRCMPLT (sprcmplt): Spare Operation Complete. Set by hardware once operation is complete. Bit is cleared by hardware when a new operation is enabled. **Note:** Just before MC release the HA block prior to the completion of the sparing operation, iMC logic will automatically update the corresponding RIR_RNK_TGT target to reflect new DST_RANK.
0:0	RO_V	0x0	SPRINPROGRESS (sprinprogress): Spare Operation in progress. This bit is set by hardware once operation has started. It is cleared once operation is complete or fails.

2.2.5 scrubaddresslo

Scrub Address Low.

This register contains part of the address of the last patrol scrub request issued. When running memtest, the failing address is logged in this register on memtest errors. Software can write the next address to be scrubbed into this register. The STARTSCRUB bit will then trigger the specified address to be scrubbed. Patrol scrubs must be disabled to reliably write this register.

Type: CFG Bus: 1 Offset: 0x98		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
30:0	RW_LBV	0x0	RANKADD (rankadd): Contains the rank address of the last scrub issued. Can be written to specify the next scrub address with STARTSCRUB. Patrol Scrubs must be disabled when writing to this field.

2.2.6 scrubaddresshi

Scrub Address High.

This register pair contains part of the address of the last patrol scrub request issued. Software can write the next address into this register. Scrubbing must be disabled to reliably read and write this register. The STARTSCRUB bit will then trigger the specified address to be scrubbed.

Type: CFG Bus: 1 Offset: 0x9c		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
11:10	RW_LBV	0x0	CHNL (chnl): Can be written to specify the next scrub address with STARTSCRUB. This register is updated with channel address of the last scrub address issued. Patrol Scrubs must be disabled when writing to this field.
7:4	RW_LBV	0x0	RANK (rank): Contains the physical rank ID of the last scrub issued. Can be written to specify the next scrub address with STARTSCRUB. Patrol Scrubs must be disabled when writing to this field.

2.2.7 scrubctl

This register contains the Scrub control parameters and status.

Type: CFG Bus: 1 Offset: 0xa0		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
31:31	RW_L	0x0	Scrub Enable (scrub_en): Scrub Enable when set.
30:30	RW_LB	0x0	Stop on complete (stop_on_cmpl): Stop patrol scrub at end of memory range. This mode is meant to be used as part of memory migration flow. Intel SMI is signaled by default.
29:29	RW_LBV	0x0	patrol range complete (ptl_cmpl): When stop_on_cmpl is enabled, patrol will stop at the end of the address range and set this bit. Patrol will resume from beginning of address range when this bit or stop_on_cmpl is cleared by BIOS and patrol scrub is still enabled by scrub_en.
28:28	RW_LB	0x0	Stop on error (stop_on_err): Stop patrol scrub on poison or uncorrectable. On poison, patrol will log error then stop. On uncorr, patrol will convert to poison if enabled then stop. This mode is meant to be used as part of memory migration flow. Intel SMI is signaled by default.
27:27	RW_LBV	0x0	patrol stopped (ptl_stopped): When stop_on_err is set, patrol will stop on error and set this bit. Patrol will resume at the next address when this bit or stop_on_err is cleared by BIOS and patrol scrub is still enabled by scrub_en.
26:26	RW_LBV	0x0	SCRUBISSUED (scrubissued): When Set, the scrub address registers contain the last scrub address issued.
25:25	RW_LB	0x0	ISSUEONCE (issueonce): When Set, the patrol scrub engine will issue the address in the scrub address registers only once and stop.

Type: CFG Bus: 1 Offset: 0xa0		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
24:24	RW_LBV	0x0	STARTSCRUB (startscrub): When Set, the Patrol scrub engine will start from the address in the scrub address registers. Once the scrub is issued this bit is reset.
23:0	RW_LB	0x0	SCRUBINTERVAL (scrubinterval): Defines the interval in DCLKS between patrol scrub requests. The calculation for this register to get a scrub to every line in 24 hours is: ((86400)/(memory capacity/64))/cycle time of DCLK. RESTRICTIONS: Can only be changed when patrol scrubs are disabled. Set to a minimum value of 1500

2.2.8 spareinterval

Defines the interval between normal and sparing operations. Interval is defined in dclk.

Type: CFG Bus: 1 Offset: 0xa8		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
28:16	RW-LB	0x320	NUMSPARE (numspare): Sparing operation duration. System requests will be blocked during this interval and only sparing copy operations will be serviced.
15:0	RW-LB	0xc80	NORMAL OPERATION DURATION (normopdur): Normal operation duration. System requests will be serviced during this interval.

2.2.9 rasenables

RAS Enables Register

Type: CFG Bus: 1 Offset: 0xac		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
0:0	RW_LB	0x0	MIRROREN (mirroren): Mirror mode enable. The channel mapping must be set up before this bit will have an effect on iMC operation. This changes the error policy.

2.2.10 smisparectl

System Management Interrupt and Spare control register.

Type: CFG Bus: 1 Offset: 0xb4		PortID: N/A Device: 19,22	Function: 1
Bit	**Attr**	**Default**	**Description**
17:17	RW-LB	0x0	INTRPT_SEL_PIN (intrpt_sel_pin): Enable pin signaling. When set the interrupt is signaled via the ERROR_N[0] pin to get the attention of a BMC.
16:16	RW-LB	0x0	INTRPT_SEL_CMCI (intrpt_sel_cmci): (CMCI used as a proxy for NMI signaling). Set to enable NMI signaling. Clear to disable NMI signaling. If both NMI and Intel SMI enable bits are set then only Intel SMI is sent.
15:15	RW-LB	0x0	INTRPT_SEL_SMI (intrpt_sel_smi): Intel SMI enable. Set to enable Intel SMI signaling. Clear to disable Intel SMI signaling.

2.2.11 leaky_bucket_cfg

The leaky bucket is implemented as a 53-bit DCLK counter. The upper 42-bit of the 53-bit counter is captured in LEAKY_BUCKET_CNTR_LO and LEAKY_BUCKET_CNTR_HI registers. The carry “strobe” from the not-shown least significant 11-bit counter will trigger this 42-bit counter-pair to count. LEAKY_BUCKET_CFG contains two hot encoding thresholds LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO. The 42-bit counter-pair is compared with the two thresholds pair specified by LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO.

Type: CFG	PortID: N/A	
Bus: 1	Device: 19,22	Function: 1
Offset: 0xb8		

Bit	Attr	Default	Description
11:6	RW	0x0	LEAKY_BKT_CFG_HI (leaky_bkt_cfg_hi): This is the higher order bit select mask of the two hot encoding threshold. The value of this field specify the bit position of the mask: 00h: reserved 01h: LEAKY_BUCKET_CNTR_LO bit 1, i.e. bit 12 of the full 53b counter ... 1Fh: LEAKY_BUCKET_CNTR_LO bit 31, i.e. bit 42 of the full 53b counter 20h: LEAKY_BUCKET_CNTR_HI bit 0, i.e. bit 43 of the full 53b counter ... 29h: LEAKY_BUCKET_CNTR_HI bit 9, i.e. bit 52 of the full 53b counter 2Ah - 3F: reserved When both counter bits selected by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO are set, the 53b leaky bucket counter will be reset and the logic will generate a primary leak Strobe which is used by a 2-bit LEAKY_BKT_2ND_CNTR. LEAKY_BKT_2ND_CNTR_LIMIT specifies the value to generate LEAK pulse which is used to decrement the correctable error counter by 1 as shown below: LEAKY_BKT_2ND_CNTR_LIMIT LEAK pulse to decrement CE counter by 1 00b (default): 4 x Primary leak strobe (four times the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) 01b: 1x Primary leak strobe (same as the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) 10b: 2x Primary leak strobe (two times the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) 11b: 3x Primary leak strobe (two times the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) ***Note:*** A value of all zeroes in LEAKY_BUCKET_CFG register is equivalent to no leaky bucketing. BIOS must program this register to any non-zero value before switching to NORMAL mode.

Type: CFG	PortID: N/A		
Bus: 1	Device: 19,22	Function: 1	
Offset: 0xb8			
Bit	**Attr**	**Default**	**Description**
5:0	RW	0x0	LEAKY_BKT_CFG_LO (leaky_bkt_cfg_lo): This is the lower order bit select mask of the two hot encoding threshold. The value of this field specify the bit position of the mask: 00h: reserved 01h: LEAKY_BUCKET_CNTR_LO bit 1, i.e. bit 12 of the full 53b counter ... 1Fh: LEAKY_BUCKET_CNTR_LO bit 31, i.e. bit 42 of the full 53b counter 20h: LEAKY_BUCKET_CNTR_HI bit 0, i.e. bit 43 of the full 53b counter ... 29h: LEAKY_BUCKET_CNTR_HI bit 9, i.e. bit 52 of the full 53b counter 2Ah - 3F: reserved When both counter bits selected by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO are set, the 53b leaky bucket counter will be reset and the logic will generate a primary leak Strobe which is used by a 2-bit LEAKY_BKT_2ND_CNTR. LEAKY_BKT_2ND_CNTR_LIMIT specifies the value to generate LEAK pulse which is used to decrement the correctable error counter by 1 as shown below: LEAKY_BKT_2ND_CNTR_LIMIT LEAK pulse to decrement CE counter by 1 00b (default): 4 x Primary leak strobe (four times the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) 01b: 1x Primary leak strobe (same as the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) 10b: 2x Primary leak strobe (two times the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) 11b: 3x Primary leak strobe (two times the value programmed by the LEAKY_BKT_CFG_HI and LEAKY_BKT_CFG_LO) ***Note:*** A value of all zeroes in LEAKY_BUCKET_CFG register is equivalent to no leaky bucketing MRC BIOS must program this register to any non-zero value before switching to NORMAL mode.

2.2.12 leaky_bucket_cntr_lo

Type: CFG	PortID: N/A		
Bus: 1	Device: 19,22	Function: 1	
Offset: 0xc0			
Bit	**Attr**	**Default**	**Description**
31:0	RW_V	0x0	Leaky Bucket Counter Low (leaky_bkt_cntr_lo): This is the lower half of the leaky bucket counter. The full counter is actually a 53b “DCLK” counter. There is a least significant 11b of the 53b counter is not captured in CSR. The carry “strobe” from the not-shown least significant 11b counter will trigger this 42b counter pair to count. The 42b counter-pair is compared with the two-hot encoding threshold specified by the LEAKY_BUCKET_CFG_HI and LEAKY_BUCKET_CFG_LO pair. When the counter bits specified by the LEAKY_BUCKET_CFG_HI and LEAKY_BUCKET_CFG_LO are both set, the 53b counter is reset and the leaky bucket logic will generate a LEAK strobe last for 1 DCLK.

2.2.13 leaky_bucket_cntr_hi

Type: CFG Bus: 1 Offset: 0xc4	PortID: N/A Device: 19,22	Function: 1	
Bit	**Attr**	**Default**	**Description**
9:0	RW_V	0x0	Leaky Bucket Counter High Limit (leaky_bkt_cntr_hi): This is the upper half of the leaky bucket counter. The full counter is actually a 53b “DCLK” counter. There is a least significant 11b of the 53b counter is not captured in CSR. The carry “strobe” from the not-shown least significant 11b counter will trigger this 42b counter pair to count. The 42b counter-pair is compared with the two-hot encoding threshold specified by the LEAKY_BUCKET_CFG_HI and LEAKY_BUCKET_CFG_LO pair. When the counter bits specified by the LEAKY_BUCKET_CFG_HI and LEAKY_BUCKET_CFG_LO are both set, the 53b counter is reset and the leaky bucket logic will generate a LEAK strobe last for 1 DCLK.

2.3 Device 19,22 Functions 2,3,4,5

DID		VID		0h	DIMMMTR_0	80h
PCISTS		PCICMD		4h	DIMMMTR_1	84h
CCR			RID	8h	DIMMMTR_2	88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h		90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		A0h
				24h		A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h		B0h
			CAPPTR	34h		B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
PXPCAP				40h		C0h
				44h		C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h		D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
				68h		E8h
				6Ch		ECh
				70h		F0h

	74h		F4h
	78h		F8h
	7Ch		FCh

2.3.1 pxpcap

Type: CFG Bus: 1 Offset: 0x40		PortID: N/A Device: 19,22	Function: 2,3,4,5
Bit	**Attr**	**Default**	**Description**
29:25	RO	0x0	Interrupt Message Number (interrupt_message_number): NA for this device
24:24	RO	0x0	Slot Implemented (slot_implemented): NA for integrated endpoints
23:20	RO	0x9	Device/Port Type (device_port_type): Device type is Root Complex Integrated Endpoint
19:16	RO	0x1	Capability Version (capability_version): PCI Express Capability is Compliant with Version 1.0 of the PCI Express Spec. ***Note:*** This capability structure is not compliant with Versions beyond 1.0, since they require additional capability registers to be reserved. The only purpose for this capability structure is to make enhanced configuration space available. Minimizing the size of this structure is accomplished by reporting version 1.0 compliancy and reporting that this is an integrated root port device. As such, only three Dwords of configuration space are required for this structure.
15:8	RO	0x0	Next Capability Pointer (next_ptr): Pointer to the next capability. Set to 0 to indicate there are no more capability structures.
7:0	RO	0x10	Capability ID (capability_id): Provides the PCI Express capability ID assigned by PCI-SIG.

2.3.2 dimmmtr_[0:2]

DIMM Memory Technology.

Type: CFG Bus: 1 Offset: 0x80, 0x84, 0x88		PortID: N/A Device: 19,22	Function: 2,3,4,5
Bit	**Attr**	**Default**	**Description**
22:22	RW_LB	0x0	hdrl_parity: When set, will enable parity calculation to include address bits 17:16 which are sent on chip select lines 7:6 and 3:2.
21:21	RW_LB	0x0	hdrl: When set, will enable High Density Reduced Load mode which will transmit Row address bits 17:16 on chip select lines 7:6 and 3:2.
20:20	RW_LB	0x0	ddr4_mode: When set, indicating DDR4 DIMM type is used. Channel 0 and 1, and channel 2 and 3 must have matching values even if both DDR channels are not populated.
19:16	RW_LB	0x0	RANK_DISABLE control (rank_disable): RANK Disable Control to disable patrol, refresh and ZQCAL operation. When set, no patrol or refresh will be performed on this rank. ODT termination is not affected by this bit.

Type: CFG Bus: 1 Offset: 0x80, 0x84, 0x88	PortID: N/A Device: 19,22		Function: 2,3,4,5
Bit	**Attr**	**Default**	**Description**
14:14	RW_LB	0x0	DIMM_POP (dimm_pop): DIMM populated if set; otherwise, unpopulated. If none of the fields from dimmmtr_0/1/2 is set, DDRIO DLL will not be enabled.
13:12	RW_LB	0x0	RANK_CNT (rank_cnt): 00 - SR 01 - DR 10 - QR 11 - 8R
9:8	RW_LB	0x0	DDR3_WIDTH (ddr3_width): 00 - x4 01 - x8 10 - x16 11 - reserved Used to determine if a configuration is capable of supporting DDDC.
6:5	RW_LB	0x0	DDR3_DNSTY (ddr3_dnsty): 00 - Reserved 01 - 2 Gb 10 - 4 Gb 11 - 8 Gb
4:2	RW_LB	0x0	RA_WIDTH (ra_width): 000 - reserved 001 - 13 bits 010 - 14 bits 011 - 15 bits 100 - 16 bits 101 - 17 bits 110 - 18 bits 111: reserved
1:0	RW_LB	0x0	CA_WIDTH (ca_width): 00 - 10 bits 01 - 11 bits 10 - 12 bits 11 - reserved

2.3.3 pxpenhcap

This field points to the next Capability in extended configuration space.

Type: CFG **Bus:** 1 **Offset:** 0x100		**PortID:** N/A **Device:** 19,22	**Function:** 2,3,4,5
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x0	Next Capability Offset (next_capability_offset):
19:16	RO	0x0	Capability Version (capability_version): Indicates there are no capability structures in the enhanced configuration space.
15:0	RO	0x0	Capability ID (capability_id): Indicates there are no capability structures in the enhanced configuration space.

2.4 Device 20,21,23,24 Functions 0, 1

DID		VID		0h		80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h		90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		
				24h		A0h
				28h		A4h
SDID		SVID		2Ch		A8h
				30h		ACh
			CAPPTR	34h		B0h
				38h		B4h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		B8h
PXPCAP				40h		BCh
				44h		C0h
				48h		C4h
				4Ch		
				50h		
				54h		D0h
				58h		D4h
				5Ch		D8h
				60h		DCh
				64h		E0h
				68h		E4h
				6Ch		E8h
				70h		F0h

	74h		F4h
	78h		F8h
	7Ch		FCh

	100h			180h
	104h			184h
CHN_TEMP_CFG	108h			188h
CHN_TEMP_STAT	10Ch			18Ch
DIMM_TEMP_OEM_0	110h	THRT_PWR_DIMM_1	THRT_PWR_DIMM_0	190h
DIMM_TEMP_OEM_1	114h		THRT_PWR_DIMM_2	194h
DIMM_TEMP_OEM_2	118h			198h
	11Ch			19Ch
DIMM_TEMP_TH_0	120h			1A0h
DIMM_TEMP_TH_1	124h			1A4h
DIMM_TEMP_TH_2	128h			1A8h
	12Ch			1ACh
DIMM_TEMP_THRT_LMT_0	130h			1B0h
DIMM_TEMP_THRT_LMT_1	134h			1B4h
DIMM_TEMP_THRT_LMT_2	138h			1B8h
	13Ch			1BCh
DIMM_TEMP_EV_OFST_0	140h			1C0h
DIMM_TEMP_EV_OFST_1	144h			1C4h
DIMM_TEMP_EV_OFST_2	148h			1C8h
	14Ch			1CCh
DIMMTEMPSTAT_0	150h			1D0h
DIMMTEMPSTAT_1	154h			1D4h
DIMMTEMPSTAT_2	158h			1D8h
	15Ch			1DCh
	160h			1E0h
	164h			1E4h
	168h			1E8h
	16Ch			1ECh
	170h			1F0h
	174h			1F4h
	178h			1F8h
	17Ch			1FCh

2.4.1 pxpcap

Type: CFG Bus: 1 Offset: 0x40		PortID: N/A Device: 20,21,23,24	Function: 0,1
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x10	Capability ID (capability_id): Provides the PCI Express capability ID assigned by PCI-SIG.

2.4.2 chn_temp_cfg

Type: CFG Bus: 1 Offset: 0x108		PortID: N/A Device: 20,21,23,24	Function: 0,1
Bit	**Attr**	**Default**	**Description**
31:31	RW	0x1	OLTT_EN (oltt_en): Enable OLTT temperature tracking.
29:29	RW	0x0	CLTT_OR_PCODE_TEMP_MUX_SEL (cltt_or_pcode_temp_mux_sel): The TEMP_STAT byte update mux select control to direct the source to update DIMMTEMPSTAT_[0:3][7:0]: 0: Corresponding to the DIMM TEMP_STAT byte from PCODE_TEMP_OUTPUT. 1: TSOD temperature reading from CLTT logic.
28:28	RW_O	0x1	CLTT_DEBUG_DISABLE_LOCK (cltt_debug_disable_lock): Lock bit of DIMMTEMPSTAT_[0:3][7:0]:Set this lock bit to disable configuration write to DIMMTEMPSTAT_[0:3][7:0].
27:27	RW	0x1	Enables thermal bandwidth throttling limit (bw_limit_thrt_en):
23:16	RW	0x0	THRT_EXT (thrt_ext): Max number of throttled transactions to be issued during BWLIMITTF due to externally asserted MEMHOT#.
15:15	RW	0x0	THRT_ALLOW_ISOCH (thrt_allow_isoch): When this bit is zero, MC will lower CKE during Thermal Throttling, and ISOCH is blocked. When this bit is one, MC will NOT lower CKE during Thermal Throttling, and ISOCH will be allowed base on bandwidth throttling setting. However, setting this bit would mean more power consumption due to CKE is asserted during thermal or power throttling.
10:0	RW	0x3ff	BW_LIMIT_TF (bw_limit_tf): BW Throttle Window Size in DCLK. Note: This value is left shifted 3 bits before being used.

2.4.3 chn_temp_stat

Type: CFG Bus: 1 Offset: 0x10c		PortID: N/A Device: 20,21,23,24	Function: 0,1
Bit	**Attr**	**Default**	**Description**
3:3	RW1C	0x0	Event Asserted MXB (ev_asrt_mxb): Event Asserted on Scalable Memory Buffer
2:2	RW1C	0x0	Event Asserted on DIMM ID 2 (ev_asrt_dimm2): Event Asserted on DIMM ID 2

Type: CFG Bus: 1 Offset: 0x10c	PortID: N/A Device: 20,21,23,24		Function: 0,1
Bit	**Attr**	**Default**	**Description**
1:1	RW1C	0x0	Event Asserted on DIMM ID 1 (ev_asrt_dimm1): Event Asserted on DIMM ID 1
0:0	RW1C	0x0	Event Asserted on DIMM ID 0 (ev_asrt_dimm0): Event Asserted on DIMM ID 0

2.4.4 dimm_temp_oem_[0:2]

Type: CFG Bus: 1 Offset: 0x110, 0x114, 0x118	PortID: N/A Device: 20,21,23,24		Function: 0,1
Bit	**Attr**	**Default**	**Description**
26:24	RW	0x0	TEMP_OEM_HI_HYST (temp_oem_hi_hyst): Positive going Threshold Hysteresis Value. This value is subtracted from TEMPOEMHI to determine the point where the asserted status for that threshold will clear. Set to 00h if sensor does not support positive-going threshold hysteresis
18:16	RW	0x0	TEMP_OEM_LO_HYST (temp_oem_lo_hyst): Negative going Threshold Hysteresis Value. This value is added to TEMPOEMLO to determine the point where the asserted status for that threshold will clear. Set to 00h if sensor does not support negative-going threshold hysteresis.
15:8	RW	0x50	TEMP_OEM_HI (temp_oem_hi): Upper Threshold value - TCase threshold at which to Initiate System Interrupt (Intel SMI or MEMHOT#) at a+ going rate. ***Note:*** The default value is listed in decimal. Valid range: 32 - 127 in degree (C). Others: reserved.
7:0	RW	0x4b	TEMP_OEM_LO (temp_oem_lo): Lower Threshold Value - TCase threshold at which to Initiate System Interrupt (Intel SMI or MEMHOT#) at a - going rate. Note: the default value is listed in decimal. Valid range: 32 - 127 in degree (C). Others: reserved.

2.4.5 dimm_temp_th_[0:2]

Type: CFG Bus: 1 Offset: 0x120, 0x124, 0x128	PortID: N/A Device: 20,21,23,24		Function: 0,1
Bit	**Attr**	**Default**	**Description**
26:24	RW-LB	0x0	TEMP_THRT_HYST (temp_thrt_hyst): Positive going Threshold Hysteresis Value. Set to 00h if sensor does not support positive-going threshold hysteresis. This value is subtracted from TEMP_THRT_XX to determine the point where the asserted status for that threshold will clear.

Type: CFG	PortID: N/A		
Bus: 1	Device: 20,21,23,24	Function: 0,1	
Offset: 0x120, 0x124, 0x128			
Bit	**Attr**	**Default**	**Description**
23:16	RW-LB	0x5f	TEMP_HI (temp_hi): TCase threshold at which to Initiate THRTCRIT and assert THERMTRIP# valid range: 32 - 127 in degree (C). Note: the default value is listed in decimal. FF: Disabled Others: reserved. TEMP_HI should be programmed so it is greater than TEMP_MID.
15:8	RW	0x5a	TEMP_MID (temp_mid): TCase threshold at which to Initiate THRTHI and assert valid range: 32 - 127 in degree (C). ***Note:*** The default value is listed in decimal. FF: Disabled Others: reserved. TEMP_MID should be programmed so it is less than TEMP_HI.
7:0	RW	0x55	TEMP_LO (temp_lo): TCase threshold at which to Initiate 2x refresh andor THRTMID and initiate Interrupt (MEMHOT#). ***Note:*** The default value is listed in decimal.valid range: 32 - 127 in degree (C). FF: Disabled Others: reserved. TEMP_LO should be programmed so it is less than TEMP_MID

2.4.6 dimm_temp_thrt_lmt_[0:2]

All three THRT_CRIT, THRT_HI and THRT_MID are per DIMM BW limit, i.e. all activities (ACT, READ, WRITE) from all ranks within a DIMM are tracked together in one DIMM activity counter.

Type: CFG	PortID: N/A		
Bus: 1	Device: 20,21,23,24	Function: 0,1	
Offset: 0x130, 0x134, 0x138			
Bit	**Attr**	**Default**	**Description**
23:16	RW-LB	0x0	THRT_CRIT (thrt_crit): Max number of throttled transactions (ACT, READ, WRITE) to be issued during BWLIMITTF.
15:8	RW-LB	0xf	THRT_HI (thrt_hi): Max number of throttled transactions (ACT, READ, WRITE) to be issued during BWLIMITTF.
7:0	RW	0xff	THRT_MID (thrt_mid): Max number of throttled transactions (ACT, READ, WRITE) to be issued during BWLIMITTF.

2.4.7 dimm_temp_ev_ofst_[0:2]

Type: CFG Bus: 1 Offset: 0x140, 0x144, 0x148		PortID: N/A Device: 20,21,23,24	Function: 0,1
Bit	**Attr**	**Default**	**Description**
31:24	RO	0x0	TEMP_AVG_INTRVL (temp_avg_intrvl): Temperature data is averaged over this period. At the end of averaging period (ms) , averaging process starts again. 0x1 - 0xFF Averaging data is read via TEMPDIMM STATUSREGISTER (Byte 1/2) as well as used for generating hysteresis based interrupts. 00 Instantaneous Data (non-averaged) is read via TEMPDIMM STATUSREGISTER (Byte 1/2) as well as used for generating hysteresis based interrupts. Note: Cpu does not support temp averaging.
14:14	RW	0x0	Initiate THRTMID on TEMPLO (ev_thrtmid_templo): Initiate THRTMID on TEMPLO
13:13	RW	0x1	Initiate 2X refresh on TEMPLO (ev_2x_ref_templo_en): Initiate 2X refresh on TEMPLO DIMM with extended temperature range capability will need double refresh rate in order to avoid data lost when DIMM temperature is above 85C but below 95C. ***Warning***: If the 2x refresh is disable with extended temperature range DIMM configuration, system cooling and power thermal throttling scheme must guarantee the DIMM temperature will not exceed 85C.
12:12	RW	0x0	Assert MEMHOT Event on TEMPHI (ev_mh_temphi_en): Assert MEMHOT# Event on TEMPHI
11:11	RW	0x0	Assert MEMHOT Event on TEMPMID (ev_mh_tempmid_en): Assert MEMHOT# Event on TEMPMID
10:10	RW	0x0	Assert MEMHOT Event on TEMPLO (ev_mh_templo_en): Assert MEMHOT# Event on TEMPLO
9:9	RW	0x0	Assert MEMHOT Event on TEMPOEMHI (ev_mh_tempoemhi_en): Assert MEMHOT# Event on TEMPOEMHI
8:8	RW	0x0	Assert MEMHOT Event on TEMPOEMLO (ev_mh_tempoemlo_en): Assert MEMHOT# Event on TEMPOEMLO
3:0	RW	0x0	DIMM_TEMP_OFFSET (dimm_temp_offset): Temperature Offset Register.

2.4.8 dimmtempstat_[0:2]

Type: CFG Bus: 1 Offset: 0x150, 0x154, 0x158		PortID: N/A Device: 20,21,23,24	Function: 0,1
Bit	**Attr**	**Default**	**Description**
28:28	RW1C	0x0	Event Asserted on TEMPHI going HIGH (ev_asrt_temphi): Event Asserted on TEMPHI going HIGH It is assumed that each of the event assertion is going to trigger Configurable interrupt (Either MEMHOT# only or both Intel SMI and MEMHOT#) defined in bit 30 of CHN_TEMP_CFG
27:27	RW1C	0x0	Event Asserted on TEMPMID going High (ev_asrt_tempmid): Event Asserted on TEMPMID going High It is assumed that each of the event assertion is going to trigger configurable interrupt (Either MEMHOT# only or both Intel SMI and MEMHOT#) defined in bit 30 of CHN_TEMP_CFG

Type: CFG	PortID: N/A	
Bus: 1	Device: 20,21,23,24	Function: 0,1
Offset: 0x150, 0x154, 0x158		

Bit	Attr	Default	Description
26:26	RW1C	0x0	Event Asserted on TEMPLO Going High (ev_asrt_templo): Event Asserted on TEMPLO Going High It is assumed that each of the event assertion is going to trigger Configurable interrupt (Either MEMHOT# only or both Intel SMI and MEMHOT#) defined in bit 30 of CHN_TEMP_CFG
25:25	RW1C	0x0	Event Asserted on TEMPOEMLO Going Low (ev_asrt_tempoemlo): Event Asserted on TEMPOEMLO Going Low It is assumed that each of the event assertion is going to trigger Configurable interrupt (Either MEMHOT# only or both Intel SMI and MEMHOT#) defined in bit 30 of CHN_TEMP_CFG
24:24	RW1C	0x0	Event Asserted on TEMPOEMHI Going High (ev_asrt_tempoemhi): Event Asserted on TEMPOEMHI Going High It is assumed that each of the event assertion is going to trigger Configurable interrupt (Either MEMHOT# only or both Intel SMI and MEMHOT#) defined in bit 30 of CHN_TEMP_CFG
7:0	RW_LV	0x55	DIMM_TEMP (dimm_temp): Current DIMM Temperature for thermal throttling. Lock by CLTT_DEBUG_DISABLE_LOCK. When the CLTT_DEBUG_DISABLE_LOCK is set, this field becomes read-only, i.e. configuration write to this byte is aborted. This byte is updated from internal logic from a 2:1 Mux which can be selected from either CLTT temperature or from the corresponding temperature registers output (PCODE_TEMP_OUTPUT) updated from microcode. The mux select is controlled by CLTT_OR_PCODE_TEMP_MUX_SEL defined in CHN_TEMP_CFG register. Valid range from 0 to 127 i.e. 0C to +127C. Any negative value read from TSOD is forced to 0. TSOD decimal point value is also truncated to integer value.

2.4.9 thrt_pwr_dimm_[0:2]

bit[10:0]: Max number of transactions (ACT, READ, WRITE) to be allowed during the 1 usec throttling timeframe per power throttling.

Type: CFG	PortID: N/A	
Bus: 1	Device: 20,21,23,24	Function: 0,1
Offset: 0x190, 0x192, 0x194		

Bit	Attr	Default	Description
15:15	RW	0x1	THRT_PWR_EN (thrt_pwr_en): bit[15]: set to one to enable the power throttling for the DIMM.
11:0	RW	0xfff	Power Throttling Control (thrt_pwr): bit[11:0]: Max number of transactions (ACT, READ, WRITE) to be allowed (per DIMM) during the 1 micro-sec throttling timeframe per power throttling.

2.5 Device 20,21,23,24 Functions 2, 3

DID		VID		0h		80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h		90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		A0h
				24h		A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h		B0h
			CAPPTR	34h		B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
PXPCAP				40h		C0h
				44h		C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h		D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
				68h		E8h
				6Ch		ECh
				70h		F0h
				74h		F4h
				78h		F8h
				7Ch		FCh

	100h		180h
CORRERRCNT_0	104h		184h
CORRERRCNT_1	108h		188h
CORRERRCNT_2	10Ch		18Ch
CORRERRCNT_3	110h		190h
	114h		194h
	118h		198h
CORRERRTHRSHLD_0	11Ch		19Ch

CORRERRTHRSHLD_1				120h		1A0h
CORRERRTHRSHLD_2				124h		1A4h
CORRERRTHRSHLD_3				128h		1A8h
				12Ch		1ACh
				130h		1B0h
CORRERRORSTATUS				134h		1B4h
LEAKY_BKT_2ND_CNTR_REG				138h		1B8h
				13Ch		1BCh
DEVTAG_CNTL_3	DEVTAG_CNTL_2	DEVTAG_CNTL_1	DEVTAG_CNTL_0	140h		1C0h
DEVTAG_CNTL_7	DEVTAG_CNTL_6	DEVTAG_CNTL_5	DEVTAG_CNTL_4	144h		1C4h
				148h		1C8h
				14Ch		1CCh
				150h		1D0h
				154h		1D4h
				158h		1D8h
				15Ch		1DCh
				160h		1E0h
				164h		1E4h
				168h		1E8h
				16Ch		1ECh
				170h		1F0h
				174h		1F4h
				178h		1F8h
				17Ch		1FCh

2.5.1 correrrcnt_0

Per Rank corrected error counters.

Type: CFG Bus: 1 Offset: 0x104		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
31:31	RW1CS	0x0	RANK 1 OVERFLOW (overflow_1): The corrected error count for this rank has been overflowed. Once set it can only be cleared via a write from BIOS.
30:16	RWS_LV	0x0	RANK 1 CORRECTABLE ERROR COUNT (cor_err_cnt_1): The corrected error count for this rank. Hardware automatically clears this field when the corresponding OVERFLOW_x bit is changing from 0 to 1.
15:15	RW1CS	0x0	RANK 0 OVERFLOW (overflow_0): The corrected error count for this rank has been overflowed. Once set it can only be cleared via a write from BIOS.
14:0	RWS_LV	0x0	RANK 0 CORRECTABLE ERROR COUNT (cor_err_cnt_0): The corrected error count for this rank. Hardware automatically clear this field when the corresponding OVERFLOW_x bit is changing from 0 to 1.

2.5.2 correrrcnt_1

Per Rank corrected error counters.

Type: CFG Bus: 1 Offset: 0x108	PortID: N/A Device: 20,21,23,24	Function: 2,3	
Bit	**Attr**	**Default**	**Description**
31:31	RW1CS	0x0	RANK 3 OVERFLOW (overflow_3): The corrected error count has crested over the limit for this rank. Once set it can only be cleared via a write from BIOS.
30:16	RWS_LV	0x0	RANK 3 COR_ERR_CNT (cor_err_cnt_3): The corrected error count for this rank.
15:15	RW1CS	0x0	RANK 2 OVERFLOW (overflow_2): The corrected error count has crested over the limit for this rank. Once set it can only be cleared via a write from BIOS.
14:0	RWS_LV	0x0	RANK 2 COR_ERR_CNT (cor_err_cnt_2): The corrected error count for this rank.

2.5.3 correrrcnt_2

Per Rank corrected error counters.

Type: CFG Bus: 1 Offset: 0x10c	PortID: N/A Device: 20,21,23,24	Function: 2,3	
Bit	**Attr**	**Default**	**Description**
31:31	RW1CS	0x0	RANK 5 OVERFLOW (overflow_5): The corrected error count has crested over the limit for this rank. Once set it can only be cleared via a write from BIOS.
30:16	RWS_LV	0x0	RANK 5 COR_ERR_CNT (cor_err_cnt_5): The corrected error count for this rank.
15:15	RW1CS	0x0	RANK 4 OVERFLOW (overflow_4): The corrected error count has crested over the limit for this rank. Once set it can only be cleared via a write from BIOS.
14:0	RWS_LV	0x0	RANK 4 COR_ERR_CNT (cor_err_cnt_4): The corrected error count for this rank.

2.5.4 correrrcnt_3

Per Rank corrected error counters.

Type: CFG Bus: 1 Offset: 0x110		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
31:31	RW1CS	0x0	RANK 7 OVERFLOW (overflow_7): The corrected error count for this rank.
30:16	RWS_LV	0x0	RANK 7 COR_ERR_CNT_7 (cor_err_cnt_7): The corrected error count for this rank.
15:15	RW1CS	0x0	RANK 6 OVERFLOW (overflow_6): The corrected error count has crested over the limit for this rank. Once set it can only be cleared via a write from BIOS.
14:0	RWS_LV	0x0	RANK 6 COR_ERR_CNT (cor_err_cnt_6): The corrected error count for this rank.

2.5.5 correrrthrshld_0

This register holds the per rank corrected error thresholding value.

Type: CFG Bus: 1 Offset: 0x11c		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
30:16	RW-LB	0x7fff	RANK 1 COR_ERR_TH (cor_err_th_1): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.
14:0	RW-LB	0x7fff	RANK 0 COR_ERR_TH (cor_err_th_0): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.

2.5.6 correrrthrshld_1

This register holds the per rank corrected error thresholding value.

Type: CFG Bus: 1 Offset: 0x120		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
30:16	RW-LB	0x7fff	RANK 3 COR_ERR_TH (cor_err_th_3): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.
14:0	RW-LB	0x7fff	RANK 2 COR_ERR_TH (cor_err_th_2): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.

2.5.7 correrrthrshld_2

This register holds the per rank corrected error thresholding value.

Type: CFG Bus: 1 Offset: 0x124		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
30:16	RW-LB	0x7fff	RANK 5 COR_ERR_TH (cor_err_th_5): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.
14:0	RW-LB	0x7fff	RANK 4 COR_ERR_TH (cor_err_th_4): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.

2.5.8 correrrthrshld_3

This register holds the per rank corrected error thresholding value.

Type: CFG Bus: 1 Offset: 0x128		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
30:16	RW-LB	0x7fff	RANK 7 COR_ERR_TH (cor_err_th_7): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.
14:0	RW-LB	0x7fff	RANK 6 COR_ERR_TH (cor_err_th_6): The corrected error threshold for this rank that will be compared to the per rank corrected error counter.

2.5.9 correrrorstatus

Per rank corrected error status. These bits are reset by BIOS.

Type: CFG Bus: 1 Offset: 0x134		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
7:0	RW1C	0x0	ERR_OVERFLOW_STAT (err_overflow_stat): This 8 bit field is the per rank error over-threshold status bits. The organization is as follows: Bit 0 : Rank 0 Bit 1 : Rank 1 Bit 2 : Rank 2 Bit 3 : Rank 3 Bit 4 : Rank 4 Bit 5 : Rank 5 Bit 6 : Rank 6 Bit 7 : Rank 7 ***Note:*** The register tracks which rank has reached or exceeded the corresponding CORRERRTHRSHLD threshold settings.

2.5.10 leaky_bkt_2nd_cntr_reg

Type: CFG Bus: 1 Offset: 0x138		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
31:16	RW	0x0	LEAKY_BKT_2ND_CNTR_LIMIT(leaky_bkt_2nd_cntr_limit): Secondary Leaky Bucket Counter Limit (2b per DIMM). This register defines secondary leaky bucket counter limit for all 8 logical ranks within channel. The counter logic will generate the secondary LEAK pulse to decrement the rank's correctable error counter by 1 when the corresponding rank leaky bucket rank counter roll over at the predefined counter limit. The counter increment at the primary leak pulse from the LEAKY_BUCKET_CNTR_LO and LEAKY_BUCKET_CNTR_HI logic. Bit[31:30]: Rank 7 Secondary Leaky Bucket Counter Limit Bit[29:28]: Rank 6 Secondary Leaky Bucket Counter Limit Bit[27:26]: Rank 5 Secondary Leaky Bucket Counter Limit Bit[25:24]: Rank 4 Secondary Leaky Bucket Counter Limit Bit[23:22]: Rank 3 Secondary Leaky Bucket Counter Limit Bit[21:20]: Rank 2 Secondary Leaky Bucket Counter Limit Bit[19:18]: Rank 1 Secondary Leaky Bucket Counter Limit Bit[17:16]: Rank 0 Secondary Leaky Bucket Counter Limit The value of the limit is defined as the following: 0: the LEAK pulse is generated one DCLK after the primary LEAK pulse is asserted. 1: the LEAK pulse is generated one DCLK after the counter roll over at 1. 2: the LEAK pulse is generated one DCLK after the counter roll over at 2. 3: the LEAK pulse is generated one DCLK after the counter roll over at 3.

Type: CFG Bus: 1 Offset: 0x138		PortID: N/A Device: 20,21,23,24	Function: 2,3
Bit	**Attr**	**Default**	**Description**
15:0	RW_V	0x0	LEAKY_BKT_2ND_CNTR (leaky_bkt_2nd_cntr): Per rank secondary leaky bucket counter (2b per rank) bit [15:14]: rank 7 secondary leaky bucket counter bit [13:12]: rank 6 secondary leaky bucket counter bit [11:10]: rank 5 secondary leaky bucket counter bit [9:8]: rank 4 secondary leaky bucket counter bit [7:6]: rank 3 secondary leaky bucket counter bit [5:4]: rank 2 secondary leaky bucket counter bit [3:2]: rank 1 secondary leaky bucket counter bit [1:0]: rank 0 secondary leaky bucket counter

2.5.11 devtag_cntl_[0:7]

SDDC Usage model

When the number of correctable errors (CORRERRCNT_x) from a particular rank exceeds the corresponding threshold (CORRERRTHRSHLD_y), hardware will generate a Intel® Scalable Memory Interconnect (Intel® SMI) interrupt and log and preserve the failing device in the FailDevice field. SMM software will read the failing device on the particular rank. Software then set the EN bit to enable substitution of the failing device/ rank with the parity from the rest of the devices in line.

For independent channel configuration, each rank can tag once. Up to 8 ranks can be tagged.

For lock-step channel configuration, only one x8 device can be tagged per rank-pair. SMM software must identify which channel should be tagged for this rank and only set the valid bit for the channel from the channel-pair.

There is no hardware logic to report incorrect programming error. Unpredictable error and or silent data corruption will be the consequence of such programming error.

If the rank-sparing is enabled, it is recommended to prioritize the rank-sparing before triggering the device tagging due to the nature of the device tagging would drop the correction capability and any subsequent ECC error from this rank would cause uncorrectable error.

Type: CFG	PortID: N/A		
Bus: 1	Device: 20,21,23,24	Function: 2,3	
Offset: 0x140, 0x141, 0x142, 0x143, 0x144, 0x145, 0x146, 0x147			
Bit	**Attr**	**Default**	**Description**
7:7	RWS_L	0x0	Device tagging enable for this rank (en): Device tagging SDDC enable for this rank. Once set, the parity device of the rank is used for the replacement device content. After tagging, the rank will no longer have the “correction” capability. ECC error “detection” capability will not degrade after setting this bit. For lock-step channel configuration, only one x8 device can be tagged per rank-pair. SMM software must identify which channel should be tagged for this rank and only set the corresponding DEVTAG_CNTL_x.EN bit for the channel contains the fail device. The DEVTAG_CNTL_x.EN on the other channel of the corresponding rank must not be set. DDDC: On DDDC supported systems, BIOS has the option to enable SDDC in conjunction with DDDC_CNTL:SPARING to enable faster sparing with SDDC substitution. This field is cleared by HW on completion of DDDC sparing.
5:0	RWS_V	0x3f	Fail Device ID for this rank (faildevice): Hardware will capture the fail device ID of the rank in the FailDevice field upon successful correction from the device correction engine. After SDDC is enabled HW may not update this field. Valid Range is decimal 0-17 to indicate which x4 device (independent channel) or x8 device (lock-step mode) has failed.

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3 Intel® QuickPath Interconnect (Intel® QPI) Agent Registers

The Intel® QuickPath Interconnect (Intel® QPI) Agent is a is the coherent communication interface between processors.

- The Intel® Xeon® processor E7 v4 product family implements 3 Intel QPI links (0,1,2).

3.1 Device 8,9,10 Function 0

DID		VID		0h		80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h		90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		A0h
				24h		A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h		B0h
			CAPPTR	34h		B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
				40h		C0h
				44h		C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h	QPIMISCSTAT	D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
				68h		E8h
				6Ch		ECh
				70h		F0h

	74h		F4h
	78h		F8h
	7Ch		FCh

3.1.1 QPIMISCSTAT: Intel QPI Misc Status

This is a status register for Common logic in Intel QPI. It is shared between Intel QPI 0 and Intel QPI 1 in device 8, and Intel QPI 2 value is stored in device 10.

QPIMISCSTAT Bus: 1		Device: 8,10	Function: 0 Offset: D4
Bit	**Attr**	**Default**	**Description**
2:0	RO-V	011b	**Intel QPI Rate** This reflects the current Intel QPI rate setting into the PLL. 011 - 6.4 GT/s 100 - 7.2 GT/s 101 - 8 GT/s 111 - 9.6 GT/s other - Reserved

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4 Processor Utility Box (UBOX) Registers

The UBOX is the piece of processor logic that deals with the non mainstream flows in the system. This includes transactions like the register accesses, interrupt flows, lock flows and events. In addition, the UBOX houses coordination for the performance architecture, and also houses scratchpad and semaphore registers.

4.1 Device 16 Function 5

DID		VID		0h		80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h		90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		A0h
				24h		A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h		B0h
			CAPPTR	34h		B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
CPUNODEID				40h		C0h
				44h		C4h
IntControl				48h		C8h
				4Ch		CCh
				50h		D0h
GIDNIDMAP				54h		D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
UBOXErrSts				64h		E4h
				68h		E8h
				6Ch		ECh
				70h		F0h

	74h		F4h
	78h		F8h
	7Ch		FCh

4.1.1 CPUNODEID

Node ID Configuration Register

Type: CFG Bus: 1 Offset: 0x40		Port ID: N/A Device: 16	Function: 5
Bit	**Attr**	**Default**	**Description**
12:10	RW_LB	0x0	NodeID of the legacy socket(LgcNodeId): NodeID of the legacy socket.
7:5	RW_LB	0x0	NodeID of the lock master(LockNodeId): NodeID of the lock master.
2:0	RW_LB	0x0	NodeID of the local register(LclNodeId): NodeID of the local Socket.

4.1.2 IntControl

Interrupt Configuration Register

Type: CFG Bus: 1 Offset: 0x48		Port ID: N/A Device: 16	Function: 5
Bit	**Attr**	**Default**	**Description**
18:18	RW_LB	0x0	IA32 Logical Flat or Cluster Mode Override Enable(LogFlatClustOvrEn): 0: IA32 Logical Flat or Cluster Mode bit is locked as Read only bit. 1: IA32 Logical Flat or Cluster Mode bit may be written by SW, values written by xTPR update are ignored. For one time override of the IA-32 Logical Flat or Cluster Mode value, return this bit to it's default state after the bit is changed. Leaving this bit as '1' will prevent automatic update of the filter.
17:17	RW_LBV	0x0	IA32 Logical Flat or Cluster Mode(LogFltClustMod): Set by BIOS to indicate if the OS is running logical flat or logical cluster mode. This bit can also be updated by IntPrioUpd messages. This bit reflects the setup of the filter at any given time. 0 - flat, 1 - cluster.
16:16	RW_LB	0x0	Cluster Check Sampling Mode(ClastChkSmpMod): 0: Disable checking for Logical_APICID[31:0] being non-zero when sampling flat cluster mode bit in the IntPrioUpd message as part of setting bit 1 in this register 1: Enable the above checking

Type: CFG Bus: 1 Offset: 0x48		Port ID: N/A Device: 16	Function: 5
Bit	**Attr**	**Default**	**Description**
10:8	RW_LB	0x0	Vecor Based Hashe Mode Control(HashModCtr): Indicates the hash mode control for the interrupt control. Select the hush function for the Vector based Hash Mode interrupt redirection control: 000 select bits 7:4 / 5:4 for vector cluster / flat algorithm 001 select bits 6:3 / 4:3 010 select bits 4:1 / 2:1 011 select bits 3:0 / 1:0 other - reserved
6:4	RW_LB	0x0	Redirection Mode Select for Logical Interrupts(RdrModSel): Selects the redirection mode used for MSI interrupts with lowest-priority delivery mode. The following schemes are used: 000: Fixed priority 001: Round-robin 010: Interrupt vector hash.
1:1	RW_LB	0x0	Force to X2 APIC Mode(ForceX2APIC): Write: 1: Forces the system to move into X2APIC Mode. 0: No affect
0:0	RW_LB	0x1	Extended APIC Enable(xApicEn): 1: Extended XAPIC configuration. This bit can be written directly, and can also be updated using XTPR messages.

4.1.3 GIDNIDMAP

Node ID Mapping Register. Mapping between group id and NodeID

Type: CFG Bus: 1 Offset: 0x54		Port ID: N/A Device: 16	Function: 5
Bit	**Attr**	**Default**	**Description**
23:21	RW_LB	0x0	NodeID 7(NodeId7): NodeID for group id 7
20:18	RW_LB	0x0	NodeID 6(NodeId6): NodeID for group 6
17:15	RW_LB	0x0	NodeID 5(NodeId5): NodeID for group 5
14:12	RW_LB	0x0	NodeID 4(NodeId4): NodeID for group id 4
11:9	RW_LB	0x0	NodeID 3(NodeId3): NodeID for group 3
8:6	RW_LB	0x0	NodeID 2(NodeID2): NodeID for group Id 2
5:3	RW_LB	0x0	NodeID 1(NodeId1): NodeID for group Id 1
2:0	RW_LB	0x0	NodeID 0(NodeId0): NodeID for group 0

4.1.4 UBOXErrSts

This is error status register in the UBOX and covers most of the interrupt related errors.

Type: CFG Bus: 1 Offset: 0x64		Port ID: N/A Device: 16	Function: 5
Bit	**Attr**	**Default**	**Description**
16:16	RW_V	0x0	Intel SMI delivery valid(SMI_delivery_valid): Intel SMI interrupt delivery status valid, write 1'b1 to clear valid status
7:7	RWS_V	0x0	MasterLock Timeout received by UBOX(MasterLockTimeOut): Master Lock Timeout received by UBOX
6:6	RWS_V	0x0	Intel SMI Timeout received by UBOX(SMITimeOut): Intel SMI Timeout received by UBOX
5:5	RWS_V	0x0	MMCFG Write Address Misalignment received by UBOX(CFGWrAddrMisAligned): MMCFG Write Address Misalignment received by UBOX
4:4	RWS_V	0x0	MMCFG Read Address Misalignment received by UBOX(CFGRdAddrMisAligned): MMCFG Read Address Misalignment received by UBOX
3:3	RWS_V	0x0	Unsupported Opcode received by UBOX(UnsupportedOpcode): Unsupported opcode received by UBOX
2:2	RWS_V	0x0	Poison was received by UBOX(PoisonRsvd): UBOX received a poisoned transaction
1:1	RWS_V	0x0	Intel SMI source iMC(SMISrciMC): Intel SMI is caused due to an indication from the iMC
0:0	RWS_V	0x0	Intel SMI is caused due to a locally generated UMC(SMISrcUMC): This is a bit that indicates that an Intel SMI was caused due to a locally generated UMC

4.2 Device 16 Function 7

DID		VID		0h	80h
PCISTS		PCICMD		4h	84h
CCR			RID	8h	88h
BIST	HDR	PLAT	CLSR	Ch	8Ch
				10h	90h
				14h	94h
				18h	98h
				1Ch	9Ch
				20h	A0h
				24h	A4h
				28h	A8h
SDID		SVID		2Ch	ACh
				30h	B0h
			CAPPTR	34h	B4h
				38h	B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch	BCh
				40h	C0h

	44h		C4h
	48h		C8h
	4Ch		CCh
	50h	CPUBUSNO	D0h
	54h		D4h
	58h	SMICtrl	D8h
	5Ch		DCh
	60h		E0h
	64h		E4h
	68h		E8h
	6Ch		ECh
	70h		F0h
	74h		F4h
	78h		F8h
	7Ch		FCh

4.2.1 CPUBUSNO

Bus Number Configuration for the Intel® Xeon® processor E7 v4 product family.

Type: CFG Bus: 1 Offset: 0xd0	Port ID: N/A Device: 16	Function: 7	
Bit	**Attr**	**Default**	**Description**
31:31	RW_LB	0x0	Valid: Indicates whether the bus numbers have been initialized or not
15:8	RW_LB	0x0	CPU Bus Number 1(CPUBUSNO1): Bus Number for non IIO devices in the uncore in the processor.
7:0	RW_LB	0x0	CPU Bus Number 0(CPUBUSNO0): Bus Number for IIO devices in the processor.

4.2.2 SMICtrl

SMI generation control

Type: CFG Bus: 1 Offset: 0xd8			Port ID: N/A Device: 16 Function: 7
Bit	**Attr**	**Default**	**Description**
28:28	RW_LB	0x0	Disable Generation of Intel SMI from CSMI from MsgCh(SMIDis4): Disable Generation of Intel SMI from CSMI from MsgCh
27:27	RW_LB	0x0	Disable Generation of Intel SMI for new Ubox erros(SMIDis3): Disable generation of Intel SMI from message channel
26:26	RW_LB	0x1	Disable Generation of Intel SMI for new Ubox erros(SMIDis2): Disable generation of Intel SMI for lock timeout, cfg write mis-align access, and cfg read mis-align access.
25:25	RW_LB	0x0	Disable Generation of Intel SMI (all)(SMIDis): Disable generation of Intel SMI
24:24	RW_LB	0x0	UMC Intel SMI Enable (UMCSMIEn): This is the enable bit that enables Intel SMI generation due to a UMC 1 - Generate Intel SMI after the threshold counter expires. 0 - Disable generation of Intel SMI
19:0	RW_LB	0x0	Intel SMI generation threshold (Threshold): This is the countdown that happens in the hardware before an Intel SMI is generated due to a UMC.

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5 Power Controller Unit (PCU) Registers

The Power Controller Unit (PCU) is a dedicated controller that provides power and thermal management for the processor.

5.1 Device 30 Function 0

DID		VID		0h		80h
PCISTS		PCICMD		4h	PACKAGE_POWER_SKU	84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch	PACKAGE_POWER_SKU_UNIT	8Ch
				10h	PACKAGE_ENERGY_STATUS	90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		A0h
				24h		A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h		B0h
			CAPPTR	34h		B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
				40h		C0h
				44h		C4h
				48h	Package_Temperature	C8h
				4Ch		CCh
				50h		D0h
				54h	PCU_REFERENCE_CLOCK	D4h
				58h		D8h
				5Ch		DCh
MEM_TRML_TEMPERATURE_REPORT				60h		E0h
MEM_ACCUMULATED_BW_CH_0				64h	TEMPERATURE_TARGET	E4h
MEM_ACCUMULATED_BW_CH_1				68h		E8h
MEM_ACCUMULATED_BW_CH_2				6Ch		ECh
MEM_ACCUMULATED_BW_CH_3				70h		F0h
				74h		F4h
				78h		F8h
				7Ch		FCh
DID		VID		0h		80h

5.1.1 MEM_TRML_TEMPERATURE_REPORT

This register is used to report the thermal status of the memory.

The channel max temperature field is used to report the maximal temperature of all ranks.

Type: CFG Bus: 1 Offset: 0x60		Port ID: N/A Device: 30	Function: 0
Bit	**Attr**	**Default**	**Description**
31:24	RO_V	0x0	Channel 3 Maximum Temperature(Channel3_Max_Temperature): Temperature in Degrees (C).
23:16	RO_V	0x0	Channel 2 Maximum Temperature(Channel2_Max_Temperature): Temperature in Degrees (C).
15:8	RO_V	0x0	Channel 1 Maximum Temperature(Channel1_Max_Temperature): Temperature in Degrees (C).
7:0	RO_V	0x0	Channel 0 Maximum Temperature(Channel0_Max_Temperature): Temperature in Degrees (C).

5.1.2 MEM_ACCUMULATED_BW_CH_[0:3]

This register contains a measurement proportional to the weighted DRAM BW for the channel including all ranks. The weights are configured in the memory controller channel register PM_CMD_PWR.

Type: CFG Bus: 1 Offset: 0x64, 0x68, 0x6c, 0x70		Port ID: N/A Device: 30	Function: 0
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	Data(DATA): The weighted BW value is calculated by the memory controller based on the following formula: NumPrecharge * PM_CMD_PWR[PWR_RAS_PRE] + NumReads * PM_CMD_PWR[PWR_CAS_R] + NumWrites * PM_CMD_PWR[PWR_CAS_W]

5.1.3 PACKAGE_POWER_SKU

Defines allowed SKU power and timing parameters.

Type: CFG Bus: 1 Offset: 0x84		Port ID: N/A Device: 30	Function: 0
Bit	**Attr**	**Default**	**Description**
54:48	RO_V	0x12	Maximal Time Window(PKG_MAX_WIN): The maximal time window allowed for the SKU. Higher values will be clamped to this value. x = PKG_MAX_WIN[54:53] y = PKG_MAX_WIN[52:48] The timing interval window is Floating Point number given by 1.x * power(2,y). The unit of measurement is defined in PACKAGE_POWER_SKU_UNIT_MSR[TIME_UNIT].
46:32	RO_V	0x240	Maximal Package Power(PKG_MAX_PWR): The maximal package power setting allowed for the SKU. Higher values will be clamped to this value. The maximum setting is typical not guaranteed. The units for this value are defined in PACKAGE_POWER_SKU_UNIT_MSR[PWR_UNIT].
30:16	RO_V	0x60	Minimal Package Power(PKG_MIN_PWR): The minimal package power setting allowed for the SKU. Lower values will be clamped to this value. The minimum setting is typical not guaranteed. The units for this value are defined in PACKAGE_POWER_SKU_UNIT_MSR[PWR_UNIT].
14:0	RO_V	0x118	TDP Package Power(PKG_TDP): The TDP package power setting allowed for the SKU. The TDP setting is typical not guaranteed. The units for this value are defined in PACKAGE_POWER_SKU_UNIT_MSR[PWR_UNIT].

5.1.4 PACKAGE_POWER_SKU_UNIT

Defines units for calculating SKU power and timing parameters.

Type: CFG Bus: 1 Offset: 0x8c		Port ID: N/A Device: 30	Function: 0
Bit	**Attr**	**Default**	**Description**
19:16	RO_V	0xa	Time Unit(TIME_UNIT): Time Units used for power control registers. The actual unit value is calculated by 1 / Power(2,TIME_UNIT) second. The default value of 0Ah corresponds to 976 usec.
12:8	RO_V	0xe	Energy Units(ENERGY_UNIT): Energy Units used for power control registers. The actual unit value is calculated by 1 / Power(2,ENERGY_UNIT) J.
3:0	RO_V	0x3	Power Units(PWR_UNIT): Power Units used for power control registers. The actual unit value is calculated by 1 / Power(2,PWR_UNIT) W. The default value of 0011b corresponds to 18 W.

5.1.5 PACKAGE_ENERGY_STATUS

Package energy consumed by the core and uncore. The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Type: CFG Bus: 1 Offset: 0x90			Port ID: N/A Device: 30 Function: 0
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	Energy Value(DATA): Energy Value

5.1.6 Package_Temperature

Package temperature in degrees (C). This field is updated by FW.

Type: CFG Bus: 1 Offset: 0xc8			Port ID: N/A Device: 30 Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	Temperature(DATA): Package temperature in degrees (C).

5.1.7 TEMPERATURE_TARGET

Legacy register holding temperature related constants for Platform use. This register is updated by FW.

Type: CFG Bus: 1 Offset: 0xe4			Port ID: N/A Device: 30 Function: 0
Bit	**Attr**	**Default**	**Description**
27:24	RO_V	0x0	Max TCC Offset (MAX_TCC_OFFSET): Temperature offset in degrees (C) from the Processor Hot. Used for throttling temperature. Will not impact temperature reading. If offset is allowed and set, the throttle will occur and reported at lower than Processor Hot.
23:16	RO_V	0x0	Thermal Monitor Reference Temperature(REF_TEMP): This field indicates the maximum junction temperature, also referred to as the throttle temperature, TCC activation temperature or prochot temperature. This is the temperature at which the Thermal Monitor is activated.
15:8	RO_V	0x0	Fan Temperature target offset(FAN_TEMP_TARGET_OFST): Fan Temperature target offset a.k.a. T-Control. Indicates the relative offset from the Thermal Monitor Trip Temperature at which fans should be engaged.

5.2 Device 30 Function 1

DID		VID		0h		80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h		88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h		90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h		A0h
				24h	CSR_DESIRED_CORES	A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h		B0h
			CAPPTR	34h		B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
				40h		C0h
				44h		C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h		D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
SSKPD				68h		E8h
				6Ch		ECh
				70h		F0h
C2C3TT				74h		F4h
				78h		F8h
				7Ch		FCh

5.2.1 SSKPD

Sticky Scratchpad Data.

This register holds 64 writable bits with no functionality behind them.

Type: CFG Bus: 1 Offset: 0x68		Port ID: N/A Device: 30	Function: 1
Bit	**Attr**	**Default**	**Description**
63:0	RWS	0x0	Scratchpad Data(SKPD): 4 WORDs of data storage.

5.2.2 C2C3TT

C2 to C3 Transition Timer. BIOS can update this value during run-time. Unit for this register is usec with a range of 0-4095 us.

Type: CFG Bus: 1 Offset: 0x74			PortID: N/A Device: 30Function:1
Bit	**Attr**	**Default**	**Description**
11:0	RW	0x32	Pop Down Initialization Value(PPDN_INIT): Value in micro-seconds.

5.2.3 CSR_DESIRED_CORES

Number of cores/threads BIOS wants to exist on the next reset. A processor reset must be used for this register to take effect. Note, programming this register to a value higher than the product has cores should not be done.

This register is reset only by PWRGOOD.

Type: CFG Bus: 1 Offset: 0xa4		Port ID: N/A Device: 30	Function: 1
Bit	**Attr**	**Default**	**Description**
31:31	RWS_KL	0x0	Lock(LOCK): Once written to a '1', changes to this register cannot be done. Cleared only by a power-on reset
30:30	RWS_L	0x0	SMT Disable (SMT_DISABLE): Disable simultaneous multi-threading in all cores if this bit is set to '1'.
23:0	RWS_L	0x0	Cores Off Mask (CORE_OFF_MASK): BIOS will set this bit to request that the matching core should not be activated coming out of reset. The default value of this registers means that all cores are enabled. Restrictions: At least one core needs to be left active. Otherwise, FW will ignore the setting altogether.

5.3 Device 30 Function 2

DID		VID		0h		80h
PCISTS		PCICMD		4h		84h
CCR			RID	8h	PACKAGE_RAPL_PERF_STATUS	88h
BIST	HDR	PLAT	CLSR	Ch		8Ch
				10h	DRAM_POWER_INFO	90h
				14h		94h
				18h		98h
				1Ch		9Ch
				20h	DRAM_ENERGY_STATUS	A0h
				24h		A4h
				28h	DRAM_ENERGY_STATUS_CH0	A8h
SDID		SVID		2Ch		ACh
				30h	DRAM_ENERGY_STATUS_CH1	B0h
			CAPPTR	34h		B4h
				38h	DRAM_ENERGY_STATUS_CH2	B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
				40h	DRAM_ENERGY_STATUS_CH3	C0h
				44h		C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h		D4h
				58h	DRAM_RAPL_PERF_STATUS	D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
				68h		E8h
				6Ch	MCA_ERR_SRC_LOG	ECh
				70h		F0h
				74h		F4h
				78h	THERMTRIP_CONFIG	F8h
				7Ch		FCh

5.3.1 PACKAGE_RAPL_PERF_STATUS

This register is used to report Package Power limit violations.

Type: CFG Bus: 1 Offset: 0x88	Port ID: N/A Device: 30	Function: 2	
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	Power Limit Throttle Counter (PWR_LIMIT_THROTTLE_CTR): Reports the number of times the Power limiting algorithm had to clip the power limit due to hitting the lowest power state available. Accumulated PACKAGE throttled time.

5.3.2 DRAM_POWER_INFO

Defines allowed DRAM power and timing parameters.

Type: CFG Bus: 1 Offset: 0x90	Port ID: N/A Device: 30	Function: 2	
Bit	**Attr**	**Default**	**Description**
63:63	RW_KL	0x0	Lock: Lock bit to lock the Register
54:48	RW_L	0x28	Maximal Time Window (DRAM_MAX_WIN): The maximal time window allowed for the DRAM. Higher values will be clamped to this value. x = PKG_MAX_WIN[54:53] y = PKG_MAX_WIN[52:48] The timing interval window is Floating Point number given by 1.x * power(2,y). ENERGY_UNIT for DRAM domain is 15.3uJ.
46:32	RW_L	0x258	Maximal Package Power (DRAM_MAX_PWR): The maximal power setting allowed for DRAM. Higher values will be clamped to this value. The maximum setting is typical (not guaranteed). ENERGY_UNIT for DRAM domain is 15.3uJ.
30:16	RW_L	0x78	Minimal DRAM Power (DRAM_MIN_PWR): The minimal power setting allowed for DRAM. Lower values will be clamped to this value. The minimum setting is typical (not guaranteed). ENERGY_UNIT for DRAM domain is 15.3uJ.
14:0	RW_L	0x118	Spec DRAM Power (DRAM_TDP): The Spec power allowed for DRAM. The TDP setting is typical (not guaranteed). ENERGY_UNIT for DRAM domain is 15.3uJ.

5.3.3 DRAM_ENERGY_STATUS

DRAM energy consumed by all the DIMMS in all the Channels. The counter will wrap around and continue counting when it reaches its limit.

ENERGY_UNIT for DRAM domain is 15.3 uJ.

Type: CFG Bus: 1 Offset: 0xa0	Port ID: N/A Device: 30	Function: 2	
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	Energy Value(DATA): Energy of the DDR plane. This counter rolls over upon an overflow and continues counting. To determine the power consumed by the DDR, BIOS/SW can read the counter at a specific interval and divide the difference by the interval time. Power = [Value(t + x) - Value(t)]/x

5.3.4 DRAM_ENERGY_STATUS_CH[0:3]

DRAM energy consumed by all the DIMMS in ChannelX (X = 0, 1, 2, 3). The counter will wrap around and continue counting when it reaches its limit.

Type: CFG Bus: 1 Offset: 0xa8, 0xb0, 0xb8, 0xc0	Port ID: N/A Device: 30	Function: 2	
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	Energy Value(DATA): Energy Value

5.3.5 DRAM_RAPL_PERF_STATUS

This register is used to report DRAM Plane Power limit violations.

Type: CFG Bus: 1 Offset: 0xd8	Port ID: N/A Device: 30	Function: 2	
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	Power Limit Throttle Counter (PWR_LIMIT_THROTTLE_CTR): Reports the number of times the Power limiting algorithm had to clip the power limit due to hitting the lowest power state available. Accumulated DRAM throttled time.

5.3.6 MCA_ERR_SRC_LOG

MCA Error Source Log.

MC Source Log is used by the PCU to log the error sources. This register is initialized to zeros during reset. The PCU will set the relevant bits when the condition they represent appears. The PCU never clears the registers-the UBox or off-die entities should clear them when they are consumed, unless their processing involves taking down the platform.

Type: CFG Bus: 1 Offset: 0xec		Port ID: N/A Device: 30	Function: 2
Bit	**Attr**	**Default**	**Description**
31:31	RWS_V	0x0	CATERR: External error: The package asserted CATERR# for any reason. It is orbit 30, bit29; functions as a Valid bit for the other two package conditions. It has no effect when a local core is associated with the error.
30:30	RWS_V	0x0	IERR: External error: The package asserted IERR.
29:29	RWS_V	0x0	MCERR: External error: The package asserted MCERR.
23:23	RWS_V	0x0	MSMI: External error: The package observed MSMI# (for any reason). It is or(bit 22, bit21); functions as a Valid bit for the other two package conditions. It has no effect when a local core is associated with the error.
22:22	RWS_V	0x0	MSMI_IERR: External error: The package observed MSMI_IERR.
21:21	RWS_V	0x0	MSMI_MCERR: External error: The package observed MSMI_MCERR.

5.3.7 THERMTRIP_CONFIG

This register is used to configure whether the Thermtrip signal only carries the processor Trip information, or does it carry the Mem trip information as well. The register will be used by HW to enable ORing of the memtrip info into the thermtrip OR tree.

Type: CFG Bus: 1 Offset: 0xf8		Port ID: N/A Device: 30	Function: 2
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x0	Enable MEM Trip(EN_MEMTRIP): If set to 1, PCU will OR in the MEMtrip information into the ThermTrip OR Tree If set to 0, PCU will ignore the MEMtrip information and ThermTrip will just have the processor indication.

5.4 Device 30 Function 3

DID		VID		0h	CAP_HDR	80h
PCISTS		PCICMD		4h	CAPID0	84h
CCR			RID	8h	CAPID1	88h
BIST	HDR	PLAT	CLSR	Ch	CAPID2	8Ch
				10h	CAPID3	90h
				14h	CAPID4	94h
				18h	CAPID5	98h
				1Ch	CAPID6	9Ch
				20h		A0h
				24h		A4h
				28h		A8h
SDID		SVID		2Ch		ACh
				30h	SMT_CONTROL	B0h
			CAPPTR	34h	RESOLVED_CORES	B4h
				38h		B8h
MAXLAT	MINGNT	INTPIN	INTL	3Ch		BCh
				40h		C0h
				44h		C4h
				48h		C8h
				4Ch		CCh
				50h		D0h
				54h		D4h
				58h		D8h
				5Ch		DCh
				60h		E0h
				64h		E4h
				68h		E8h
				6Ch		ECh
				70h		F0h
				74h		F4h
				78h		F8h
				7Ch		FCh

Note: The CSR located at offset in Device 30, Function 3, Offset 0x10 is not a Configuration Space Header and SW should not treat it as such.

5.4.1 CAP_HDR

This register is a Capability Header. It enumerates the CAPID registers available, and points to the next CAP_PTR.

Type: CFG Bus: 1 Offset: 0x80		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
27:24	RO_FW	0x1	CAPID_Version: This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO_FW	0x18	CAPID_Length: This field indicates the structure length including the header in Bytes.
15:8	RO_FW	0x0	Next_Cap_Ptr: This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO_FW	0x9	CAP_ID: This field has the value 1001b to identify the CAPID assigned by the PCI SIG for vendor dependent capability pointers.

5.4.2 CAPID0

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x84		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
31:31	RO_FW	0x0	PCLMULQ_DIS: PCLMULQ instruction disabled.
29:29	RO_FW	0x0	PECI_EN: PECI to the Processor enabled.
26:26	RO_FW	0x0	GSSE256_DIS: GSSE instructions disabled.
23:23	RO_FW	0x0	AES_DIS: AES (Advanced Encryption Standard) disabled.
20:20	RO_FW	0x0	LT_SX_EN: Intel TXT and FIT-boot enabled.
19:19	RO_FW	0x0	LT_PRODUCTION: Intel TXT enabled.
18:18	RO_FW	0x0	SMX_DIS: Intel TXT enabled.
17:17	RO_FW	0x0	VMX_DIS: VMX (Virtual-Machine Extensions) disabled.
15:15	RO_FW	0x0	VT_X3_EN: VT-x3 (Intel® Virtualization Technology) enabled.
12:12	RO_FW	0x0	HT_DIS: Multithreading disabled.
8:8	RO_FW	0x0	PRG_TDP_LIM_EN: Usage of TURBO_POWER_LIMIT MSRs enabled.
4:4	RO_FW	0x0	DE_SKTR1_EX: Set to 1 for Intel Xeon processor E7 v4 Product Family.

Type: CFG Bus: 1 Offset: 0x84		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
3:3	RO_FW	0x0	DE_SKTR_EP4S: Indicates the socket wayness of a SKU. • If CAPID0.[3]=1 and CAPID0.[2]=1 this is an EX 8S SKU. • If CAPID0.[3]=1 and CAPID0.[2]=0 this is an EX 4S SKU. • If CAPID0.[3]=0 and CAPID0.[2]=1 this is an EX 2S SKU. • If CAPID0.[3]=0 and CAPID0.[2]=0 this is an EX 1S SKU.
2:2	RO_FW	0x0	DE_SKTR_EP2S: Indicates that device is a 2S SKU.
1:1	RO_FW	0x0	DE_SKTB2_EN: Indicates that device is a 1S SKU
0:0	RO_FW	0x0	DE_SKTB2_UP: Indicates that device is a UP SKU, independent of package.

5.4.3 CAPID1

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x88		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
31:31	RO_FW	0x0	DIS_MEM_MIRROR: Disable memory channel mirroring mode. In the mirroring mode, the server maintains two identical copies of all data in memory. The contents of branch 0 (containing channel 0/1) is duplicated in the DIMMs of branch 1 (containing channel 2/3). In the event of an uncorrectable error in one of the copies, the system can retrieve the mirrored copy of the data. The use of memory mirroring means that only half of the installed memory is available to the operating system.
30:30	RO_FW	0x0	DIS_MEM_LT_SUPPORT: Intel TXT support disabled.
29:26	RO_FW	0x0	DMFC: This field controls which values may be written to the Memory Frequency Select field 6:4 of the Clocking Configuration registers. Any attempt to write an unsupported value will be ignored. [3:3] - If set, over-clocking is supported and bits 2:0 are ignored. [2:0] - Maximum allowed memory frequency. 3b110 - up to DDR-1333 (5 x 266) 3b101 - up to DDR-1600 (6 x 266) 3b100 - up to DDR-1866 (7 x 266) All others reserved
25:23	RO_FW	0x0	MEM_PA_SIZE: Physical address size supported in the core low two bits (uncore is 44 by default) 000: 46 010: 44 101: 36 110: 40 111: 39 reserved
8:8	RO_FW	0x0	rsvd

Type: CFG Bus: 1 Offset: 0x88		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
7:7	RO_FW	0x0	X2APIC_EN: Extended APIC support enabled. When set the enables the support of x2APIC (Extended APIC) in the core and uncore.
6:6	RO_FW	0x0	CPU_HOT_ADD_EN: Intel TXT - ENABLE CPU HOT ADD.
5:5	RO_FW	0x0	PWRBITS_DIS: 0b Power features activated during reset. 1b Power features (i.e. clock gating) are not activated.
4:4	RO_FW	0x0	GV3_DIS: Intel SpeedStep® Technology disabled. Does not allow for the writing of the IA32_PERF_CTL register in order to change ratios.
1:1	RO_FW	0x0	CORE_RAS_EN: Data Poisoning, MCA recovery enabled.
0:0	RO_FW	0x0	DCA_EN: DCA (Direct Cache Access) enabled.

5.4.4 CAPID2

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x8c		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
30:30	RO_FW	0x0	QPI_LINK2_DIS: When set Intel QPI link 2 will be disabled.
29:25	RO_FW	0x0	QPI_ALLOWED_CFCLK_RATIO_DIS: Allowed Intel QPI link speeds. bit 8 = 6.4GT/s 9 = 7.2GT/s bit 10 = 8.0GT/s bit 12 = 9.6GT/s
24:24	RO_FW	0x0	QPI_LINK1_DIS: Intel QPI link 1 disabled.
23:23	RO_FW	0x0	QPI_LINK0_DIS: Intel QPI link 0 disabled.
18:18	RO_FW	0x0	PCIE_DISROL: Raid-on-load disabled.
17:17	RO_FW	0x0	PCIE_DISLTSX: Intel TXT disabled.
16:16	RO_FW	0x0	PCIE_DISLT: Intel TXT disabled.
15:15	RO_FW	0x0	PCIE_DISPCIEG3: PCIe Gen 3 disabled.
14:14	RO_FW	0x0	PCIE_DISDMA: DMA engine and supporting functionality disabled.

Type: CFG Bus: 1 Offset: 0x8c		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
2:1	RO_FW	0x0	PCIE_DISx16: PCIe x16 ports disabled (limit to x8's only).
0:0	RO_FW	0x0	PCIE_DISWS: WS features such as graphics cards in PCIe slots disabled.

5.4.5 CAPID3

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x90		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
30:30	RO_FW	0x0	DISABLE_MEM_DDR4: DDR4 disabled.
29:24	RO_FW	0x0	MC2GD: Bit0: 1.35V DDR3L LVDDR disable
22:22	RO_FW	0x0	DISABLE_SMBUS_WRT: SMBUS write capability disable control. When set, SMBus write is disabled.
21:21	RO_FW	0x0	DISABLE_ROL_OR_ADR: RAID-On-LOAD disable control. When set, memory ignores ADR event. Download may change the default value after reset de-assertion.
20:20	RO_FW	0x0	DISABLE_EXTENDED_ADDR_DIMM: Extended addressing DIMM disable control. When set, DIMM with extended addressing (MA[17/16] is forced to be zero when driving MA[17:16]).
19:19	RO_FW	0x0	DISABLE_EXTENDED_LATENCY_DIMM: Extended latency DIMM disable control. When set, DIMM with extended latency is forced to CAS to be less than or equal to 14.
18:18	RO_FW	0x0	DISABLE_PATROL_SCRUB: Patrol scrub disable control. When set, rank patrol scrub is disabled.
17:17	RO_FW	0x0	DISABLE_SPARING: Sparing disable control. When set, rank sparing is disabled.
16:16	RO_FW	0x0	DISABLE_LOCKSTEP: LOCKSTEP disable control. When set, channel lockstep operation is disabled.
15:15	RO_FW	0x0	DISABLE_CLTT: CLTT disable control. When set, CLTT support is disabled by disabling TSOD polling.
14:14	RO_FW	0x0	DISABLE_UDIMM: UDIMM disable control. When set, UDIMM support is disabled by disabling address bit swizzling.
13:13	RO_FW	0x0	DISABLE_RDIMM: RDIMM disable control. When set, RDIMM support is disabled.
12:12	RO_FW	0x0	DISABLE_3N: 3N disable control. When set, 3N mode under normal operation (excluding MRS) is disabled.
11:11	RO_FW	0x0	DISABLE_DIR: DIR disable control. When set, directory is disabled.

Type: CFG Bus: 1 Offset: 0x90		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
10:10	RO_FW	0x0	DISABLE_ECC: ECC disable control. When set, ECC is disabled.
9:9	RO_FW	0x0	DISABLE_QR_DIMM: QR DIMM disable control. When set, CS signals for QR-DIMM in slot 0-1 is disabled.
8:8	RO_FW	0x0	DISABLE_4GBIT_DDR3: 4 GB disable control. When set, the address decode to the corresponding 4 Gb mapping is disabled. Note: LR-DIMM's logical device density is also limited to 4 Gb when this is set.
7:7	RO_FW	0x0	DISABLE_8GBIT_DDR3: 8 Gb or higher disable control. When set, the address decode to the corresponding 8 Gb or higher mapping is disabled. Note: LR-DIMM's logical device density is also limited to 8 Gb when this is set.
5:5	RO_FW	0x0	DISABLE_3_DPC: 3 DPC disable control. When set, CS signals for DIMM slot 2 are disabled.
4:4	RO_FW	0x0	DISABLE_2_DPC: 2 DPC disable control. When set, CS signals for DIMM slot 1-2 (i.e. slots 0 is not disabled) are disabled.
3:0	RO_FW	0x0	CHN_DISABLE: Channel disable control. When set, the corresponding memory channel is disabled. • 0000 = Intel SMI 2 enabled (EX)

5.4.6 CAPID4

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x94		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
31:31	RO_FW	0x0	Disable DRAM Power Meter (DRAM_POWER_METER_DISABLE)
30:30	RO_FW	0x0	Disable DRAM RAPL(DRAM_RAPL_DISABLE)
26:26	RO_FW	0x0	EET_ENABLE: Energy efficient turbo enabled.
25:25	RO_FW	0x0	PCPS_DISABLE: Per-core P-state disabled.
24:24	RO_FW	0x0	UFS_DISABLE: UFS (Uncore Frequency Scaling) disabled.
19:19	RO_FW	0x0	ENHANCED_MCA_DIS: Enhanced MCA disabled
14:14	RO_FW	0x0	FMA_DIS: FMA (Floating point Multiple Add) instructions disabled.
8:6	RO_FW	0x0	PHYSICAL: Physical configuration of processor. 10:configuration 2; 01:configuration 1; 00:configuration 0;

Type: CFG Bus: 1 Offset: 0x94		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
5:4	RO_FW	0x0	PROD_TYPE — Product type 00 = Intel® Xeon® Processor E7 v4 Product Family

5.4.7 CAPID5

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x98		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
30:30	RO_FW	0x0	HITME_ENABLE : Directory Cache enabled.
29:29	RO_FW	0x0	ADDR_BASED_MEM_MIRROR: Address based memory mirroring enabled
27:27	RO_FW	0x0	Intel QuickData disabled.
26:26	RO_FW	0x0	Autonomous C-state control enabled.
25:25	RO_FW	0x0	Hardware-Controlled Performance States (HWP) enabled.
24:24	RO_FW	0x0	HSW_NI_DIS New instructions except LZCNT, TZCNT, MOVBE disabled which Intel® Xeon® Processor E7 v4 Product Family disabled.
23:0	RO_FW	0x0	LLC_SLICE_EN: Enabled Cbo slices (Cbo with enabled LLC slice).

5.4.8 CAPID6

This register is a Capability Register used to expose feature support for BIOS use. Default value varies base on SKU.

Type: CFG Bus: 1 Offset: 0x9C		Port ID: N/A Device: 30	Function: 3
Bit	**Attr**	**Default**	**Description**
30:30	RO_FW	0x0	IIO_LLCCONFIG_EN: IIO to allocate in LLC enabled.
29:29	RO_FW	0x0	DE_SKT_SECONDHA: Indicates when second Home Agent and Memory Controller is enabled.
23:0	RO_FW	0x0	LLC_IA_CORE_EN: Cores enabled on SKU of the Intel® Xeon® Processor E7 v4 Product Family.

5.4.9 SMT_CONTROL

Type: CFG **Bus:** 1 **Offset:** 0xb0		**Port ID:** N/A **Device:** 30	**Function:** 3
Bit	**Attr**	**Default**	**Description**
24:24	RO_V	0x0	SMT Capability: Enabled threads in the package. 0b 1 thread 1b 2 threads
9:8	RO_V	0x0	Thread Mask (THREAD_MASK): Thread Mask indicates which threads are enabled in the core. The LSB is the enable bit for Thread 0, whereas the MSB is the enable bit for Thread 1. This field is determined by FW based on CSR_DESIRED_CORES[SMT_DISABLE] and SKU capability.

5.4.10 RESOLVED_CORES

Type: CFG **Bus:** 1 **Offset:** 0xb4		**Port ID:** N/A **Device:** 30	**Function:** 3
Bit	**Attr**	**Default**	**Description**
23:0	RO_V	0x0	CORE_MASK — The resolved IA core mask contains the functional (enabled in SKU) and non-defeatured IA cores. The mask is indexed by logical ID. It is normally contiguous, unless BIOS defeature is activated on a particular core. BSP and APIC IDs will be set by the processor based on this value. This field is determined by FW based on CSR_DESIRED_CORES[CORE_OFF_MASK].

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6 Integrated I/O (IIO) Configuration Registers

The Integrated I/O (IIO) contains the DMI2 link, PCI Express* link, Intel QuickData Technology, IOAPIC, Intel VT-d and other related logic.

- The Intel® Xeon® Processor E7 v4 includes a single x4 DMI2 link and 32 lanes of PCI Express 3.0. Device 0 is the DMI2 link, which can also operate as a PCI Express 2.0 x4 Root Port if not connected to a PCH. Device 2 is a x16 PCIe 3.0 Root Port. Device 2 is a x16 PCIe 3.0 Root Port. Device 3 is a x16 PCIe 3.0 Root Port.

6.1 Registers Overview

6.1.1 Configuration Registers (CSR)

There are two distinct CSR register spaces supported by the IIO Module.

The first one is the traditional PCI-defined configuration registers. These registers are accessed via the well known configuration transaction mechanism defined in the PCI specification and this uses the bus:device:function number concept to address a specific device's configuration space.

The second is via MMIO space for Intel® QuickData Technology, Intel VT-d, and I/OxAPIC runtime registers.

6.1.2 BDF:BAR# for Various MMIO BARs in IIO

This is needed for any entity trying to access MMIO registers in the IIO module over message channel.

Table 6-1. BDF:BAR# for Various MMIO BARs in IIO

BAR Name	B	D	F	BAR#
DMIRCBAR	DC	0	0	0
CB-BAR0	DC	4	0	0
CB-BAR1	DC	4	1	0
CB-BAR2	DC	4	2	0
CB-BAR3	DC	4	3	0
CB-BAR4	DC	4	4	0
CB-BAR5	DC	4	5	0
CB-BAR6	DC	4	6	0
CB-BAR7	DC	4	7	0
VT-d VTBAR	DC	5	0	0
I/OxAPIC-MBAR	DC	5	4	0
I/OxAPIC-ABAR	DC	5	4	1

6.1.3 Unimplemented Devices/Functions and Registers

If the IIO module receives a configuration access over message channel or directly via the JTAG mini-port, to a device/function or BAR# that does not exist in the IIO module, the IIO module will abort these accesses. Software should not attempt or rely on reads or writes to unimplemented registers or register bits.

6.1.4 PCI Vs. PCIe Device / Function

PCI devices/functions do NOT have a PCIe capability register set and do not decode offsets 100h and beyond. Accesses to 100h and beyond are master aborted by these devices. I/OxAPIC functions are PCI functions. All other functions in the IIO module are PCIe functions and these have a PCIe capability register set and also decode address offsets 100h and beyond.

6.2 Device 0 Function 0 DMI, Device 0 Function 0 PCIe, Device 1 Function 0-1, Device 2 Function 0-3 PCIe, Device 3 Function 0-3 PCIe

Device 0 Function 0 PCIe Mode - Port 0 (X4)

Device 2 - Port 2 (X16)

Device 3 - Port 3 (X16)

References to Device 1, Port 1 should be ignored in this document as the processor type does not implement this device.

Table 6-2. Function Number of Active Root Ports in Port 1(Dev#1) based on Port Bifurcation

<table>
<tr><th rowspan="2">Port Bifurcation</th><th colspan="2">Function# of Active Root Port</th></tr>
<tr><th>7:4</th><th>3:0</th></tr>
<tr><td>x8</td><td colspan="2">0</td></tr>
<tr><td>x4x4</td><td>1</td><td>0</td></tr>
</table>

Table 6-3. Function Number of Active Root Ports in Port 2(Dev#2) based on Port Bifurcation

<table>
<tr><th rowspan="2">Port Bifurcation</th><th colspan="4">Function# of Active Root Port</th></tr>
<tr><th>15:12</th><th>11:8</th><th>7:4</th><th>3:0</th></tr>
<tr><td>x16</td><td colspan="4">0</td></tr>
<tr><td>x8x8</td><td colspan="2">2</td><td colspan="2">0</td></tr>
<tr><td>x8x4x4</td><td colspan="2">2</td><td>1</td><td>0</td></tr>
<tr><td>x4x4x8</td><td>3</td><td>2</td><td colspan="2">0</td></tr>
<tr><td>x4x4x4x4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

Table 6-4. Function Number of Active Root Ports in Port 3(Dev#3) based on Port Bifurcation

Port Bifurcation	Function# of Active Root Port			
	15:12	11:8	7:4	3:0
x16	0			
x8x8	2		0	
x8x4x4	2		1	0
x4x4x8	3	2	0	
x4x4x4x4	3	2	1	0

Register Name	Offset	Size	Device 0 Function	Device 2 Function	Device 3 Function
vid	0x0	16	0	0 - 3	0 - 3
did	0x2	16	0	0 - 3	0 - 3
pcicmd	0x4	16	0	0 - 3	0 - 3
pcists	0x6	16	0	0 - 3	0 - 3
rid	0x8	8	0	0 - 3	0 - 3
ccr	0x9	24	0	0 - 3	0 - 3
clsr	0xc	8	0	0 - 3	0 - 3
plat	0xd	8	0	0 - 3	0 - 3
hdr	0xe	8	0	0 - 3	0 - 3
bist	0xf	8	0	0 - 3	0 - 3
pbus	0x18	8	0 (PCIe)	0 - 3	0 - 3
secbus	0x19	8	0 (PCIe)	0 - 3	0 - 3
subbus	0x1a	8	0 (PCIe)	0 - 3	0 - 3
iobas	0x1c	8	0 (PCIe)	0 - 3	0 - 3
iolim	0x1d	8	0 (PCIe)	0 - 3	0 - 3
secsts	0x1e	16	0 (PCIe)	0 - 3	0 - 3
mbas	0x20	16	0 (PCIe)	0 - 3	0 - 3
mlim	0x22	16	0 (PCIe)	0 - 3	0 - 3
pbas	0x24	16	0 (PCIe)	0 - 3	0 - 3
plim	0x26	16	0 (PCIe)	0 - 3	0 - 3
pbasu	0x28	32	0 (PCIe)	0 - 3	0 - 3
plimu	0x2c	32	0 (PCIe)	0 - 3	0 - 3
capptr	0x34	8	0	0 - 3	0 - 3
intl	0x3c	8	0	0 - 3	0 - 3
intpin	0x3d	8	0	0 - 3	0 - 3
bctrl	0x3e	16	0 (PCIe)	0 - 3	0 - 3
scapid	0x40	8	0 (PCIe)	0 - 3	0 - 3
snxtptr	0x41	8	0 (PCIe)	0 - 3	0 - 3
svid	0x2c	16	0 (DMI2)		
svid	0x44	16	0 (PCIe)	0 - 3	0 - 3
sdid	0x2e	16	0 (DMI2)		

Register Name	Offset	Size	Device 0 Function	Device 2 Function	Device 3 Function
sdid	0x46	16	0 (PCIe)	0 - 3	0 - 3
dmircbar	0x50	32	0		
msicapid	0x60	8	0	0 - 3	0 - 3
msinxtptr	0x61	8	0	0 - 3	0 - 3
msimsgctl	0x62	16	0	0 - 3	0 - 3
msgadr	0x64	32	0	0 - 3	0 - 3
msgdat	0x68	32	0	0 - 3	0 - 3
msimsk	0x6c	32	0	0 - 3	0 - 3
msipending	0x70	32	0	0 - 3	0 - 3
pxpcapid	0x90	8	0	0 - 3	0 - 3
pxpnxtptr	0x91	8	0	0 - 3	0 - 3
pxpcap	0x92	16	0	0 - 3	0 - 3
devcap	0x94	32	0	0 - 3	0 - 3
devctrl	0xf0	16	0 (DMI2)		
devctrl	0x98	16	0 (PCIe)	0 - 3	0 - 3
devsts	0xf2	16	0 (DMI2)		
devsts	0x9a	16	0 (PCIe)	0 - 3	0 - 3
lnkcap	0x9c	32	0	0 - 3	0 - 3
lnkcon	0x1b0	16	0 (DMI2)		
lnkcon	0xa0	16	0 (PCIe)	0 - 3	0 - 3
lnksts	0x1b2	16	0 (DMI2)		
lnksts	0xa2	16	0 (PCIe)	0 - 3	0 - 3
sltcap	0xa4	32	0 (PCIe)	0 - 3	0 - 3
sltcon	0xa8	16	0 (PCIe)	0 - 3	0 - 3
sltsts	0xaa	16	0 (PCIe)	0 - 3	0 - 3
rootcon	0xac	16	0	0 - 3	0 - 3
rootcap	0xae	16	0	0 - 3	0 - 3
rootsts	0xb0	32	0 (PCIe)	0 - 3	0 - 3
devcap2	0xb4	32	0	0 - 3	0 - 3
devctrl2	0xf8	16	0 (DMI2)		
devctrl2	0xb8	16	0 (PCIe)	0 - 3	0 - 3
lnkcap2	0xbc	32	0	0 - 3	0 - 3
lnkcon2	0x1c0	16	0 (DMI2)		
lnkcon2	0xc0	16	0 (PCIe)	0 - 3	0 - 3
lnksts2	0x1c2	16	0 (DMI2)		
lnksts2	0xc2	16	0 (PCIe)	0 - 3	0 - 3
pmcap	0xe0	32	0	0 - 3	0 - 3
pmcsr	0xe4	32	0	0 - 3	0 - 3
xpreut_hdr_ext	0x100	32	0	0 - 3	0 - 3
xpreut_hdr_cap	0x104	32	0	0 - 3	0 - 3
xpreut_hdr_lef	0x108	32	0	0 - 3	0 - 3
acscaphdr	0x110	32	0 (PCIe)	0 - 3	0 - 3

Register Name	Offset	Size	Device 0 Function	Device 2 Function	Device 3 Function
acscap	0x114	16	0 (PCIe)	0 - 3	0 - 3
acsctrl	0x116	16	0 (PCIe)	0 - 3	0 - 3
apicbase	0x140	16	0	0 - 3	0 - 3
apiclimit	0x142	16	0	0 - 3	0 - 3
vsecphdr	0x144	32	0 (DMI2)		
vshdr	0x148	32	0 (DMI2)		
errcaphdr	0x148	32	0 (PCIe)	0 - 3	0 - 3
uncerrsts	0x14c	32	0	0 - 3	0 - 3
uncerrmsk	0x150	32	0	0 - 3	0 - 3
uncerrsev	0x154	32	0	0 - 3	0 - 3
corerrsts	0x158	32	0	0 - 3	0 - 3
corerrmsk	0x15c	32	0	0 - 3	0 - 3
errcap	0x160	32	0	0 - 3	0 - 3
hdrlog0	0x164	32	0	0 - 3	0 - 3
hdrlog1	0x168	32	0	0 - 3	0 - 3
hdrlog2	0x16c	32	0	0 - 3	0 - 3
hdrlog3	0x170	32	0	0 - 3	0 - 3
rperrcmd	0x174	32	0	0 - 3	0 - 3
rperrsts	0x178	32	0	0 - 3	0 - 3
errsid	0x17c	32	0	0 - 3	0 - 3
perfctrlsts_0	0x180	32	0	0 - 3	0 - 3
perfctrlsts_1	0x184	32	0	0 - 3	0 - 3
miscctrlsts_0	0x188	32	0	0 - 3	0 - 3
miscctrlsts_1	0x18c	32	0	0 - 3	0 - 3
pcie_iou_bif_ctrl	0x190	16	0	0	0
dmictrl	0x1a0	64	0 (DMI2)		
dmists	0x1a8	32	0 (DMI2)		
ERRINJCAP	0x1d0	32	0	0 - 3	0 - 3
ERRINJHDR	0x1d4	32	0	0 - 3	0 - 3
ERRINJCON	0x1d8	16	0	0 - 3	0 - 3
ctoctrl	0x1e0	32	0	0 - 3	0 - 3
xpcorerrsts	0x200	32	0	0 - 3	0 - 3
xpcorerrmsk	0x204	32	0	0 - 3	0 - 3
xpuncerrsts	0x208	32	0	0 - 3	0 - 3
xpuncerrmsk	0x20c	32	0	0 - 3	0 - 3
xpuncerrsev	0x210	32	0	0 - 3	0 - 3
xpuncerrptr	0x214	8	0	0 - 3	0 - 3
uncedmask	0x218	32	0	0 - 3	0 - 3
coredmask	0x21c	32	0	0 - 3	0 - 3
rpedmask	0x220	32	0	0 - 3	0 - 3
xpuncedmask	0x224	32	0	0 - 3	0 - 3
xpcoredmask	0x228	32	0	0 - 3	0 - 3

Register Name	Offset	Size	Device 0 Function	Device 2 Function	Device 3 Function
xpglberrsts	0x230	16	0	0 - 3	0 - 3
xpglberrptr	0x232	16	0	0 - 3	0 - 3
pxp2cap	0x250	32		0 - 3	0 - 3
lnkcon3	0x254	32		0 - 3	0 - 3
lnerrsts	0x258	32		0 - 3	0 - 3
ln0eq	0x25c	16		0 - 3	0 - 3
ln1eq	0x25e	16		0 - 3	0 - 3
ln2eq	0x260	16		0 - 3	0 - 3
ln3eq	0x262	16		0 - 3	0 - 3
ln4eq	0x264	16		0, 2	0, 2
ln5eq	0x266	16		0, 2	0, 2
ln6eq	0x268	16		0, 2	0, 2
ln7eq	0x26a	16		0, 2	0, 2
ln8eq	0x26c	16		0	0
ln9eq	0x26e	16		0	0
ln10eq	0x270	16		0	0
ln11eq	0x272	16		0	0
ln12eq	0x274	16		0	0
ln13eq	0x276	16		0	0
ln14eq	0x278	16		0	0
ln15eq	0x27a	16		0	0

6.2.1 vid

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x0		

Bit	Attr	Default	Description
15:0	RO	0x8086	vendor_identification_number: The value is assigned by PCI-SIG to Intel.

6.2.2 did

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x2		

Bit	Attr	Default	Description
15:0	RO RO_V (Device 0 and 3 Function 0)	For Device 0 Function 0: 0x2f00 (DMI2 Mode) 0x2f01 (PCIe Mode) For Device 2: 0x2f04 (Function 0) 0x2f05 (Function 1) 0x2f06 (Function 2) 0x2f07 (Function 3) For Device 3: 0x2f08 (Function 0) 0x2f09 (Function 1) 0x2f0a (Function 2) 0x2f0b (Function 3)	device_identification_number: Device ID values vary from function to function.

6.2.3 pcicmd

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x4		

Bit	Attr	Default	Description
10:10	RW	0x0	interrupt_disable: Interrupt Disable. Controls the ability of the PCI Express port to generate INTx messages. This bit does not affect the ability of the processor to route interrupt messages received at the PCI Express port. However, this bit controls the generation of legacy interrupts to the DMI for PCI Express errors detected internally in this port (for example, Malformed TLP, CRC error, completion time out, and so forth) or when receiving RP error messages or interrupts due to Hot Plug/Power Management events generated in legacy mode within the processor. 1: Legacy Interrupt mode is disabled 0: Legacy Interrupt mode is enabled
9:9	RO	0x0	fast_back_to_back_enable: Fast Back-to-Back Enable Not applicable to PCI Express must be hardwired to 0.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x4		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
8:8	RW	0x0	serre: SERR Enable For PCI Express/DMI ports, this field enables notifying the internal core error logic of occurrence of an uncorrectable error (fatal or non-fatal) at the port. The internal core error logic of the IIO module then decides if/how to escalate the error further (pins/message, and so forth). This bit also controls the propagation of PCI Express ERR_FATAL and ERR_NONFATAL messages received from the port to the internal IIO core error logic. 1: Fatal and Non-fatal error generation and Fatal and Non-fatal error message forwarding is enabled 0: Fatal and Non-fatal error generation and Fatal and Non-fatal error message forwarding is disabled
7:7	RO	0x0	idsel_stepping_wait_cycle_control: IDSEL Stepping/Wait Cycle Control Not applicable to PCI Express must be hardwired to 0.
6:6	RW	0x0	perre: Parity Error Response For PCI Express/DMI ports, the IIO module ignores this bit and always does ECC/parity checking and signaling for data/address of transactions both to and from IIO. This bit though affects the setting of bit 8 in the PCISTS register.
5:5	RO	0x0	vga_palette_snoop_enable: Not applicable to PCI Express must be hardwired to 0.
4:4	RO	0x0	mwie: Not applicable to PCI Express must be hardwired to 0.
3:3	RO	0x0	sce: Not applicable to PCI Express must be hardwired to 0.
2:2	RW RW_L (Device 0 Function 0)	0x0	bme:
1:1	RW RW_L (Device 0 Function 0)	0x0	mse: Memory Space Enable 1: Enables a PCI Express port's memory range registers to be decoded as valid target addresses for transactions from secondary side. 0: Disables a PCI Express port's memory range registers (including the Configuration Registers range registers) to be decoded as valid target addresses for transactions from secondary side. All memory accesses received from secondary side are UR'ed.
0:0	RW RW_L (Device 0 and 3 Function 0)	0x0	iose: IO Space Enable Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

6.2.4 pcists

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x6			PortID: N/A Device: 0 Function: 0 Device: 2 Function: 0-3 Device: 3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
15:15	RW1C	0x0	dpe: Detected Parity Error This bit is set by a root port when it receives a packet on the primary side with an uncorrectable data error (including a packet with poison bit set) or an uncorrectable address/control parity error. The setting of this bit is regardless of the Parity Error Response bit (PERRE) in the PCICMD register.
14:14	RW1C	0x0	sse: Signaled System Error 1: The root port reported fatal/non-fatal (and not correctable) errors it detected on its PCI Express interface to the IIO core error logic (which might eventually escalate the error through the ERR[2:0] pins or message to cpu core or message to PCH). Note that the SERRE bit in the PCICMD register must be set for a device to report the error the IIO core error logic.Software clears this bit by writing a '1' to it. This bit is also set (when SERR enable bit is set) when a FATAL/NON-FATAL message is forwarded to the IIO core error logic. Note that the IIO internal 'core' errors (like parity error in the internal queues) are not reported via this bit. 0: The root port did not report a fatal/non-fatal error
13:13	RW1C	0x0	rma: Received Master Abort This bit is set when a root port experiences a master abort condition on a transaction it mastered on the primary interface (uncore internal bus). Note that certain errors might be detected right at the PCI Express interface and those transactions might not 'propagate' to the primary interface before the error is detected (for example, accesses to memory above TOCM in cases where the PCIe interface logic itself might have visibility into TOCM). Such errors do not cause this bit to be set, and are reported via the PCI Express interface error bits (secondary status register). Conditions that cause bit 13 to be set, include: Device receives a completion on the primary interface (internal bus of uncore) with Unsupported Request or master abort completion Status. This includes UR status received on the primary side of a PCI Express port on peer-to-peer completions also.
12:12	RW1C	0x0	rta: Received Target Abort This bit is set when a device experiences a completer abort condition on a transaction it mastered on the primary interface (uncore internal bus). Note that certain errors might be detected right at the PCI Express interface and those transactions might not 'propagate' to the primary interface before the error is detected (for example, accesses to memory above VTBAR). Such errors do not cause this bit to be set, and are reported via the PCI Express interface error bits (secondary status register). Conditions that cause bit 12 to be set, include: Device receives a completion on the primary interface (internal bus of uncore) with completer abort completion Status. This includes CA status received on the primary side of a PCI Express port on peer-to-peer completions also.
11:11	RW1C	0x0	sta: Signaled Target Abort This bit is set when a root port signals a completer abort completion status on the primary side (internal bus of uncore). This condition includes a PCI Express port forwarding a completer abort status received on a completion from the secondary.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x6		

Bit	Attr	Default	Description
10:9	RO	0x0	devsel_timing: Not applicable to PCI Express. Hardwired to 0.
8:8	RW1C	0x0	mdpe: Master Data Parity Error This bit is set by a root port if the Parity Error Response bit in the PCI Command register is set and it either receives a completion with poisoned data from the primary side or it forwards a packet with data (including MSI writes) to the primary side with poison.
7:7	RO	0x0	fast_back_to_back: Not applicable to PCI Express. Hardwired to 0.
5:5	RO	0x0	pci66mhz_capable: Not applicable to PCI Express. Hardwired to 0.
4:4	RO	0x1	capabilities_list: Not applicable to PCI Express. Hardwired to 0.
3:3	RO_V	0x0	intx_status: This Read-only bit reflects the state of the interrupt in the PCI Express Root Port. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will this device generate INTx interrupt. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.This bit does not get set for interrupts forwarded to the root port from downstream devices in the hierarchy. When MSI are enabled, Interrupt status should not be set.

6.2.5 rid

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x8		

Bit	Attr	Default	Description
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register in any Intel® Xeon® Processor E7 v4 product family function.

6.2.6 ccr

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x9		

Bit	Attr	Default	Description
23:16	RO_V	0x6	base_class: Generic Device
15:8	RO_V	0x4 0x80 (Device 3 Function 0 only)	sub_class: Generic Device
7:0	RO_V	0x0	interface: This field is hardwired to 00h for PCI Express port.

6.2.7 clsr

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0xc		

Bit	Attr	Default	Description
7:0	RW	0x0	cacheline_size: This register is set as RW for compatibility reasons only. Cacheline size is always 64B. IIO hardware ignores this setting.

6.2.8 plat

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0xd		

Bit	Attr	Default	Description
7:0	RO	0x0	primary_latency_timer: Not applicable to PCI Express. Hardwired to 00h.

6.2.9 hdr

Type: CFG	**PortID:** N/A	
Bus: 0	**Device:** 0	**Function:** 0
Bus: 0	**Device:** 2	**Function:** 0-3
Bus: 0	**Device:** 3	**Function:** 0-3
Offset: 0xe		

Bit	Attr	Default	Description
7:7	RO_V RO (Device 0 Function 0)	0x1 0x0 (Device 0 Function 0)	mfd: Multi-function Device This bit defaults to 0 for Device 0. This bit defaults to 1 for Devices 2-3. BIOS can individually control the value of this bit in Function 0 of these devices, based on HDRTYPCTRL register. BIOS will write to that register to change this field to 0 in Function 0 of these devices, if it exposes only Function 0 in the device to OS. Note: In product SKUs where only Function 0 of the device is exposed to any software (BIOS/OS), BIOS would have to still set the control bits mentioned above to set the this bit in this register to be compliant per PCI rules.
6:0	RO RO_V (Device 0 Function 0)	0x1 0x0 (Device 0 Function 0)	cl: Configuration Layout This field identifies the format of the configuration header layout. In DMI mode, default is 00h indicating a conventional type 00h PCI header. In PCIe mode, the default is 01h, corresponding to Type 1 for a PCIe root port.

6.2.10 bist

Type: CFG	**PortID:** N/A	
Bus: 0	**Device:** 0	**Function:** 0
Bus: 0	**Device:** 2	**Function:** 0-3
Bus: 0	**Device:** 3	**Function:** 0-3
Offset: 0xf		

Bit	Attr	Default	Description
7:0	RO	0x0	bist_tests: Not Supported. Hardwire to 00h.

6.2.11 pbus

Primary Bus Number Register.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0 (PCIe Mode)	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x18			

Bit	Attr	Default	Description
7:0	RW	0x0	pbn: Configuration software programs this field with the number of the bus on the primary side of the bridge. This register has to be kept consistent with the Internal Bus Number 0 in the CPUBUSNO01 register. BIOS (and OS if internal bus number gets moved) must program this register to the correct value since IIO hardware would depend on this register for inbound configuration cycle decode purposes.

6.2.12 secbus

Secondary Bus Number Register.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0 (PCIe Mode)	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x19			

Bit	Attr	Default	Description
7:0	RW	0x0	sbn: This field is programmed by configuration software to assign a bus number to the secondary bus of the virtual P2P bridge. IIO uses this register to either forward a configuration transaction as a Type 1 or Type 0 to PCI Express.

6.2.13 subbus

Subordinate Bus Number Register.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0 (PCIe Mode)	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x1a			

Bit	Attr	Default	Description
7:0	RW	0x0	subordinate_bus_number: This register is programmed by configuration software with the number of the highest subordinate bus that is behind the PCI Express port. Any transaction that falls between the secondary and subordinate bus number (both inclusive) of an Express port is forwarded to the express port.

6.2.14 iobas

I/O Base Register.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x1c		

Bit	Attr	Default	Description
7:4	RW	0xf	i_o_base_address: Corresponds to A[15:12] of the IO base address of the PCI Express port. See also the IOLIM register description.
3:2	RW_L	0x0	more_i_o_base_address: When EN1K is set in the IIOMISCCTRL register, these bits become RW and allow for 1K granularity of I/O addressing, otherwise these are RO.
1:0	RO	0x0	i_o_address_capability: IIO supports only 16 bit addressing

6.2.15 iolim

I/O Limit Register.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x1d		

Bit	Attr	Default	Description
7:4	RW	0x0	i_o_address_limit: Corresponds to A[15:12] of the I/O limit address of the PCI Express port.The I/O Base and I/O Limit registers define an address range that is used by the PCI Express port to determine when to forward I/O transactions from one interface to the other using the following formula: IO_BASE <= A[15:12] <= IO_LIMIT The bottom of the defined I/O address range will be aligned to a 4KB boundary (1KB if EN1K bit is set. Refer to the IIOMISCCTRL register for definition of EN1K bit) while the top of the region specified by IO_LIMIT will be one less than a 4 KB (1KB if EN1K bit is set) multiple. ***Notes:*** Setting the I/O limit less than I/O base disables the I/O range altogether. General the I/O base and limit registers won't be programmed by software without clearing the IOSE bit first.
3:2	RW_L	0x0	more_i_o_address_limit: When EN1K is set in the IIOMISCCTRL register, these bits become RW and allow for 1K granularity of I/O addressing, otherwise these are RO.
1:0	RO	0x0	i_o_address_limit_capability: IIO only supports 16 bit addressing

6.2.16 secsts

Secondary Status Register.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0 (PCIe Mode)	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x1e			

Bit	Attr	Default	Description
15:15	RW1C	0x0	dpe: Detected Parity Error This bit is set by the root port whenever it receives a poisoned TLP in the PCI Express port. This bit is set regardless of the state the Parity Error Response Enable bit in the Bridge Control register.
14:14	RW1C	0x0	rse: Received System Error This bit is set by the root port when it receives a ERR_FATAL or ERR_NONFATAL message from PCI Express. Note this does not include the virtual ERR* messages that are internally generated from the root port when it detects an error on its own.
13:13	RW1C	0x0	rma: Received Master Abort Status This bit is set when the root port receives a Completion with 'Unsupported Request Completion' Status or when the root port master aborts a Type0 configuration packet that has a non-zero device number.
12:12	RW1C	0x0	rta: Received Target Abort Status This bit is set when the root port receives a Completion with 'Completer Abort' Status.
11:11	RW1C	0x0	sta: Signaled Target Abort This bit is set when the root port sends a completion packet with a 'Completer Abort' Status (including peer-to-peer completions that are forwarded from one port to another).
10:9	RO	0x0	devsel_timing: Not applicable to PCI Express. Hardwired to 0.
8:8	RW1C	0x0	mdpe: Master Data Parity Error This bit is set by the root port on the secondary side (PCI Express link) if the Parity Error Response Enable bit (PERRE) is set in Bridge Control register and either of the following two conditions occurs: The PCI Express port receives a Completion from PCI Express marked poisoned. The PCI Express port poisons an outgoing packet with data. If the Parity Error Response Enable bit in Bridge Control Register is cleared, this bit is never set.
7:7	RO	0x0	fast_back_to_back_transactions_capable: Not applicable to PCI Express. Hardwired to 0.
5:5	RO	0x0	pci66_mhz_capability: Not applicable to PCI Express. Hardwired to 0.

6.2.17 mbas

Memory Base.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x20		**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	 **Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3
Bit	**Attr**	**Default**	**Description**
15:4	RW	0xfff	memory_base_address: Corresponds to A[31:20] of the 32 bit memory window's base address of the PCI Express port. See also the MLIM register description.

6.2.18 mlim

Memory Limit Register.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x22		**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	 **Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3
Bit	**Attr**	**Default**	**Description**
15:4	RW	0x0	memory_limit_address: Corresponds to A[31:20] of the 32 bit memory window's limit address that corresponds to the upper limit of the range of memory accesses that will be passed by the PCI Express bridge.The Memory Base and Memory Limit registers define a memory mapped IO non-prefetchable address range (32-bit addresses) and the IIO directs accesses in this range to the PCI Express port based on the following formula: MEMORY_BASE <= A[31:20] <= MEMORY_LIMIT The upper 12 bits of both the Memory Base and Memory Limit registers are read;/write and corresponds to the upper 12 address bits, A[31:20] of 32-bit addresses. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary and the top of the defined memory address range will be one less than a 1 MB boundary. ***Notes:*** Setting the memory limit less than memory base disables the 32-bit memory range altogether. Note that in general the memory base and limit registers won't be programmed by software without clearing the MSE bit first.

6.2.19 pbas

Prefetchable Memory Base Register.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x24**				

Bit	Attr	Default	Description
15:4	RW	0xfff	prefetchable_memory_base_address: Corresponds to A[31:20] of the prefetchable memory address range's base address of the PCI Express port. See also the PLIMU register description.
3:0	RO	0x1	prefetchable_memory_base_address_capability: IIO sets this bit to 01h to indicate 64bit capability.

6.2.20 plim

Prefetchable Memory Limit Register.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x26**				

Bit	Attr	Default	Description
15:4	RW	0x0	prefetchable_memory_limit_address: Corresponds to A[31:20] of the prefetchable memory address range's limit address of the PCI Express port. See also the PLIMU register description.
3:0	RO	0x1	prefetchable_memory_limit_address_capability: IIO sets this field to 01h to indicate 64bit capability.

6.2.21 pbasu

Prefetchable Memory Base Upper 32 bits.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x28**				

Bit	Attr	Default	Description
31:0	RW	0xffffffff	prefetchable_upper_32_bit_memory_base_address: Corresponds to A[63:32] of the prefetchable memory address range's base address of the PCI Express port. See also the PLIMU register description.

6.2.22 plimu

Prefetchable Memory Limit Upper 32 bits.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x2c	**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	**Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
31:0	RW	0x0	prefetchable_upper_32_bit_memory_limit_address: Corresponds to A[63:32] of the prefetchable memory address range's limit address of the PCI Express port.The Prefetchable Memory Base and Memory Limit registers define a memory mapped I/O prefetchable address range (64-bit addresses) which is used by the PCI Express bridge to determine when to forward memory transactions based on the following formula: PREFETCH_MEMORY_BASE_UPPER :: PREFETCH_MEMORY_BASE <= A[63:20] <= PREFETCH_MEMORY_LIMIT_UPPER :: PREFETCH_MEMORY_LIMIT The upper 12 bits of both the Prefetchable Memory Base and Memory Limit registers are read/write and corresponds to the upper 12 address bits, A[31:20] of 32-bit addresses. The bottom of the defined memory address range will be aligned to a 1 MB boundary and the top of the defined memory address range will be one less than a 1 MB boundary. The bottom 4 bits of both the Prefetchable Memory Base and Prefetchable Memory Limit registers are read-only, contain the same value, and encode whether or not the bridge supports 64-bit addresses. If these four bits have the value 0h, then the bridge supports only 32 bit addresses. If these four bits have the value 1h, then the bridge supports 64-bit addresses and the Prefetchable Base Upper 32 Bits and Prefetchable Limit Upper 32 Bits registers hold the rest of the 64-bit prefetchable base and limit addresses respectively. Setting the prefetchable memory limit less than prefetchable memory base disables the 64-bit prefetchable memory range altogether. ***Notes:*** In general the memory base and limit registers won't be programmed by software without clearing the MSE bit first.

6.2.23 capptr

Capability Pointer.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x34	**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	**Function:** 0 **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
7:0	RO_V (Device 0 Function 0, Device 2 Function 0-3) RW_V (Device 3 Function 0) RO (Device 3 Function 1-3)	0x40 0x60 (Device 3 Function 0) 0x90 (Device 0 Function 0)	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.

6.2.24 intl

Interrupt Line Register.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x3c	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
7:0	RW RO (Device 0 Function 0)	0x0	interrupt_line: N/A for these devices

6.2.25 intpin

Interrupt Pin Register.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x3d	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
7:0	RW_O	0x1	intp: N/A since these devices do not generate any interrupt on their own

6.2.26 bctrl

Bridge Control Register.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x3e	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
6:6	RW	0x0	sbr: 1: Setting this bit triggers a hot reset on the link for the corresponding PCI Express port and the PCI Express hierarchy domain subordinate to the port. This sends the LTSSM into the Training (or Link) Control Reset state, which necessarily implies a reset to the downstream device and all subordinate devices. The transaction layer corresponding to port will be emptied by virtue of the link going down when this bit is set. This means that in the outbound direction, all posted transactions are dropped and non-posted transactions are sent a UR response. In the inbound direction, completions for inbound NP requests are dropped when they arrive. Inbound posted writes are retired normally.Note also that a secondary bus reset will not reset the virtual PCI-to-PCI bridge configuration registers of the targeted PCI Express port. 0: No reset happens on the PCI Express port.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x3e	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
4:4	RW	0x0	vga16b: This bit enables the virtual PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. 0: execute 10-bit address decodes on VGA I/O accesses. 1: execute 16-bit address decodes on VGA I/O accesses. Notes: This bit only has meaning if bit 3 of this register is also set to 1, enabling VGA IO decoding and forwarding by the bridge.
3:3	RW	0x0	vgaen: Controls the routing of CPU initiated transactions targeting VGA compatible IO and memory address ranges. This bit must only be set for one p2p port in the entire system.
2:2	RW	0x0	isaen: Modifies the response by the root port to an I/O access issued by the core that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIM registers. 1: The root port will not forward to PCI Express any IO transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIM registers. 0: All addresses defined by the IOBASE and IOLIM for core issued IO transactions will be mapped to PCI Express.
1:1	RW	0x0	serre: SERR Response Enable This bit controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL messages from the PCI Express port to the primary side. 1: Enables forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL messages. 0: Disables forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL
0:0	RW	0x0	perre: Parity Error Response Enable This only effect this bit has is on the setting of bit 8 in the SECSTS register

6.2.27 scapid

Subsystem Capability Identity.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x40	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
7:0	RO RW_O (Device 0 Function 0)	0xd	capability_id: Assigned by PCI-SIG for subsystem capability ID

6.2.28 snxtptr

Subsystem ID Next Pointer.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x41**				

Bit	Attr	Default	Description
7:0	RO	0x60	next_ptr: This field is set to 60h for the next capability list MSI capability structure in the chain.

6.2.29 svid

Subsystem Vendor ID.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (DMI2 Mode)**
Offset:	**0x2c**				
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x44**				

Bit	Attr	Default	Description
15:0	RW_O	0x8086	subsystem_vendor_id: Assigned by PCI-SIG for the subsystem vendor.

6.2.30 sdid

Subsystem Identity.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (DMI2 Mode)**
Offset:	**0x2e**				
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x46**				

Bit	Attr	Default	Description
15:0	RW_O	0x0	subsystem_device_id: Assigned by the subsystem vendor to uniquely identify the subsystem.

6.2.31 dmircbar

DMI Root Complex Register Block Base Address.

Type: CFG Bus: 0 Offset: 0x50	PortID: N/A Device: 0		Function: 0
Bit	**Attr**	**Default**	**Description**
31:12	RW_LB	0x0	dmircbar: This field corresponds to bits 32 to 12 of the base address DMI Root Complex register space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 64GB of addressable memory space. System Software uses this base address to program the DMI Root Complex register set. All the Bits in this register are locked in Intel TXT mode.
0:0	RW_LB	0x0	dmircbaren: 0: DMIRCBAR is disabled and does not claim any memory 1: DMIRCBAR memory mapped accesses are claimed and decoded Notes: Accesses to registers pointed to by the DMIRCBAR, via message channel or JTAG mini-port are not gated by this enable bit i.e. accesses these registers are honored regardless of the setting of this bit.

6.2.32 msicapid

MSI Capability ID.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x60	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x5	capability_id: Assigned by PCI-SIG for MSI root ports.

6.2.33 msinxtptr

MSI Next Pointer.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x61	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
7:0	RW_O	0x90	next_ptr: This field is set to 90h for the next capability list PCI Express capability structure in the chain.

6.2.34 msimsgctl

MSI Control.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x62	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
8:8	RO	0x1	pvmc: This bit indicates that PCI Express ports support MSI per-vector masking.
7:7	RO	0x0	b64ac: This field is hardwired to 0h since the message addresses are only 32-bit addresses (for example, FEEx_xxxxh).
6:4	RW	0x0	mme: Multiple Message Enable. Applicable only to PCI Express ports. Software writes to this field to indicate the number of allocated messages which is aligned to a power of two. When MSI is enabled, the software will allocate at least one message to the device. A value of 000 indicates 1 message. Any value greater than or equal to 001 indicates a message of 2.
3:1	RO	0x1	mmc: Multiple Message Capable. Intel® Xeon® Processor E7 v4 product family's Express ports support two messages for all their internal events.
0:0	RW	0x0	msien: Software sets this bit to select INTx style interrupt or MSI interrupt for root port generated interrupts. 0: INTx interrupt mechanism is used for root port interrupts, provided the override bits in MISCCTRLSTS allow it 1: MSI interrupt mechanism is used for root port interrupts, provided the override bits in MISCCTRLSTS allow it Note there bits 4:2 and bit 2 MISCCTRLSTS can disable both MSI and INTx interrupt from being generated on root port interrupt events.

6.2.35 msgadr

The MSI Address Register (MSIAR) contains the system specific address information to route MSI interrupts from the root ports and is broken into its constituent fields.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x64	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
31:2	RW	0x0	address_id:

6.2.36 msgdat

MSI Data Register.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x68	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
15:0	RW	0x0	data:

6.2.37 msimsk

MSI Mask Bit.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x6c	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
1:0	RW	0x0	mask_bits: Relevant only when MSI is enabled and used for interrupts generated by the root port. For each Mask bit that is set, the PCI Express port is prohibited from sending the associated message. When only one message is allocated to the root port by software, only mask bit 0 is relevant and used by hardware.

6.2.38 msipending

MSI Pending Bit.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x70	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
1:0	RO_V	0x0	pending_bits: Relevant only when MSI is enabled and used for interrupts generated by the root port. When MSI is not enabled or used by the root port, this register always reads a value 0. For each Pending bit that is set, the PCI Express port has a pending associated message. When only one message is allocated to the root port by software, only pending bit 0 is setcleared by hardware and pending bit 1 always reads 0. Hardware sets this bit whenever it has an interrupt pending to be sent. This bit remains set till either the interrupt is sent by hardware or the status bits associated with the interrupt condition are cleared by software.

6.2.39 pxpcapid

PCI Express Capability Identity.

Type: CFG **Bus: 0** **Bus: 0** **Bus: 0** **Offset: 0x90**	**PortID: N/A** **Device: 0** **Device: 2** **Device: 3**	 **Function: 0** **Function: 0-3** **Function: 0-3**	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x10	capability_id: Provides the PCI Express capability ID assigned by PCI-SIG.

6.2.40 pxpnxtptr

PCI Express Next Pointer.

Type: CFG **Bus: 0** **Bus: 0** **Bus: 0** **Offset: 0x91**	**PortID: N/A** **Device: 0** **Device: 2** **Device: 3**	 **Function: 0** **Function: 0-3** **Function: 0-3**	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0xe0	next_ptr: This field is set to the PCI Power Management capability.

6.2.41 pxpcap

PCI Express Capabilities Register.

Type: CFG **Bus: 0** **Bus: 0** **Bus: 0** **Offset: 0x92**	**PortID: N/A** **Device: 0** **Device: 2** **Device: 3**	 **Function: 0** **Function: 0-3** **Function: 0-3**	
Bit	**Attr**	**Default**	**Description**
13:9	RO	0x0	interrupt_message_number: Applies to root ports. This field indicates the interrupt message number that is generated for Power Management/Hot Plug/BW-change events. When there are more than one MSI interrupt Number allocated for the root port MSI interrupts, this register field is required to contain the offset between the base Message Data and the MSI Message that is generated when there are Power Management/Hot Plug/BW-change interrupts. IIO assigns the first vector for Power Management/Hot Plug/BW-change events and so this field is set to 0.
8:8	RW_O	0x0	slot_implemented: Applies only to the root ports. 1: indicates that the PCI Express link associated with the port is connected to a slot. 0: indicates no slot is connected to this port.
7:4	RO_V	0x4	device_port_type: This field identifies the type of device. It is set to 0x4 for all the Express ports.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x92		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
3:0	RW_O	0x2	capability_version: This field identifies the version of the PCI Express capability structure, which is 2h as of now. This register field is left as RW-O to cover any unknowns with Gen3.

6.2.42 devcap

The PCI Express Device Capabilities register identifies device specific information for the device.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x94		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
27:26	RO	0x0	captured_slot_power_limit_scale: Does not apply to root ports or integrated devices.
25:18	RO	0x0	captured_slot_power_limit_value: Does not apply to root ports or integrated devices.
15:15	RO	0x1	role_based_error_reporting: IIO is 1.1 compliant and so supports this feature
14:14	RO	0x0	power_indicator_present_on_device: Does not apply to root ports or integrated devices.
13:13	RO	0x0	attention_indicator_present: Does not apply to root ports or integrated devices.
12:12	RO	0x0	attention_button_present: Does not apply to root ports or integrated devices.
11:9	RO	0x0	endpoint_l1_acceptable_latency: N/A
8:6	RO	0x0	endpoint_l0s_acceptable_latency: N/A
5:5	RW_O	0x0 0x1 (Device 3 Function 0)	extended_tag_field_supported:
4:3	RO	0x0	phantom_functions_supported: IIO does not support phantom functions.
2:0	RO	0x1 0x0 (Device 0 Function 0)	max_payload_size_supported: Max payload is 128B on the DMI/PCIe port corresponding to Port 0.

6.2.43 devctrl

PCI Express Device Control.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 0	**Function:** 0 (DMI2 Mode)	
Offset: 0xf0			
Bus: 0	**Device:** 0	**Function:** 0 (PCIe Mode)	
Bus: 0	**Device:** 2	**Function:** 0-3	
Bus: 0	**Device:** 3	**Function:** 0-3	
Offset: 0x98			

Bit	Attr	Default	Description
14:12	RO	0x0	max_read_request_size: PCI Express/DMI ports in Processor do not generate requests greater than 64B and this field is RO.
11:11	RO	0x0	enable_no_snoop: Not applicable to DMI or PCIe root ports since they never set the 'No Snoop' bit for transactions they originate (not forwarded from peer) to PCI Express/DMI. This bit has no impact on forwarding of NoSnoop attribute on peer requests.
10:10	RO	0x0	auxiliary_power_management_enable: Not applicable to Processor
9:9	RO	0x0	phantom_functions_enable: Not applicable to IIO since it never uses phantom functions as a requester.
8:8	RW RO (Device 0 Function 0)	0x0	extended_tag_field_enable: N/A since IIO it never generates any requests on its own that uses tags 7:5. Note though that on peer to peer writes, IIO forwards the tag field along without modification and tag fields 7:5 could be set and that is not impacted by this bit.
7:5	RW_LV RW (Device 0 Function 0)	0x0	max_payload_size: 000: 128B max payload size 001: 256B max payload size others: alias to 128B IIO can receive packets equal to the size set by this field. IIO generate read completions as large as the value set by this field. IIO generates memory writes of max 64B.
4:4	RO	0x0	enable_relaxed_ordering: Not applicable to root/DMI ports since they never set relaxed ordering bit as a requester (this does not include tx forwarded from peer devices). This bit has no impact on forwarding of relaxed ordering attribute on peer requests.
3:3	RW	0x0	unsupported_request_reporting_enable: This bit controls the reporting of unsupported requests that IIO itself detects on requests its receives from a PCI Express/DMI port. 0: Reporting of unsupported requests is disabled 1: Reporting of unsupported requests is enabled.
2:2	RW	0x0	fatal_error_reporting_enable: Controls the reporting of fatal errors that IIO detects on the PCI Express/DMI interface. 0 = Reporting of Fatal error detected by device is disabled 1 = Reporting of Fatal error detected by device is enabled
1:1	RW	0x0	non_fatal_error_reporting_enable: Controls the reporting of non-fatal errors that IIO detects on the PCI Express/DMI interface. 0 = Reporting of Non Fatal error detected by device is disabled 1 = Reporting of Non Fatal error detected by device is enabled

Type: CFG Bus: 0 Offset: 0xf0 Bus: 0 Bus: 0 Bus: 0 Offset: 0x98	PortID: N/A Device: 0 Device: 0 Device: 2 Device: 3		Function: 0 (DMI2 Mode) Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x0	correctable_error_reporting_enable: Controls the reporting of correctable errors that IIO detects on the PCI Express/DMI interface 0 = Reporting of link Correctable error detected by the port is disabled 1 = Reporting of link Correctable error detected by port is enabled

6.2.44 devsts

PCI Express Device Status.

Type: CFG Bus: 0 Offset: 0xf2 Bus: 0 Bus: 0 Bus: 0 Offset: 0x9a	PortID: N/A Device: 0 Device: 0 Device: 2 Device: 3		Function: 0 (DMI2 Mode) Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
5:5	RO	0x0	transactions_pending: Does not apply to Root/DMI ports, that is, bit hardwired to 0 for these devices.
4:4	RO	0x0	aux_power_detected: Does not apply to the processor
3:3	RW1C	0x0	unsupported_request_detected: This bit indicates that the root port or DMI port detected an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. 1: Unsupported Request detected at the device/port. These unsupported requests are NP requests inbound that the root port or DMI port received and it detected them as unsupported requests (for example, address decoding failures that the root port detected on a packet, receiving inbound lock reads, BME bit is clear and so forth). 0: No unsupported request detected by the root or DMI port Note: This bit is not set on peer-to-peer completions with UR status that are forwarded by the root port or DMI port to the PCIe/DMI link.
2:2	RW1C	0x0	fatal_error_detected: This bit indicates that a fatal (uncorrectable) error is detected by the root or DMI port. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. 1: Fatal errors detected 0: No Fatal errors detected
1:1	RW1C	0x0	non_fatal_error_detected: This bit gets set if a non-fatal uncorrectable error is detected by the root or DMI port. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. 1: Non Fatal errors detected 0: No non-Fatal Errors detected

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0 (DMI2 Mode)	
Offset: 0xf2			
Bus: 0	Device: 0	Function: 0 (PCIe Mode)	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x9a			

Bit	Attr	Default	Description
0:0	RW1C	0x0	correctable_error_detected: This bit gets set if a correctable error is detected by the root or DMI port. Errors are logged in this register regardless of whether error reporting is enabled or not in the PCI Express Device Control register. 1: correctable errors detected 0: No correctable errors detected

6.2.45 lnkcap

PCI Express Link Capabilities

The Link Capabilities register identifies the PCI Express specific link capabilities. The link capabilities register needs some default values setup by the local host.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x9c		

Bit	Attr	Default	Description
31:24	RW_O	0x0	port_number: This field indicates the PCI Express port number for the link and is initialized by software/BIOS. IIO hardware does nothing with this bit.
22:22	RW_O	0x1	aspm_optionality_compliance:
21:21	RO_V	0x1	link_bandwidth_notification_capability: A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms.
20:20	RO	0x1	data_link_layer_link_active_reporting_capable: IIO supports reporting status of the data link layer so software knows when it can enumerate a device on the link or otherwise know the status of the link.
19:19	RO	0x1	surprise_down_error_reporting_capable: IIO supports reporting a surprise down error condition
18:18	RO	0x0	clock_power_management: Does not apply to processor
17:15	RW_O	0x2	l1_exit_latency: This field indicates the L1 exit latency for the given PCI Express port. It indicates the length of time this port requires to complete transition from L1 to L0. 000: Less than 1us 001: 1 us to less than 2 us 010: 2 us to less than 4 us 011: 4 us to less than 8 us 100: 8 us to less than 16 us 101: 16 us to less than 32 us 110: 32 us to 64 us 111: More than 64us

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x9c	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
14:12	RW_O	0x3	l0s_exit_latency: This field indicates the L0s exit latency (i.e L0s to L0) for the PCI Express port. 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 us 101: 1 is to less than 2 us 110: 2 is to 4 us 111: More than 4 us
11:10	RW_O	0x3	active_state_link_pm_support: This field indicates the level of active state power management supported on the given PCI Express port. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Supported
9:4	RW_O	0x4	maximum_link_width: This field indicates the maximum width of the given PCI Express Link attached to the port. 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16 Others: Reserved This is left as a RW-O register for bios to update based on the platform usage of the links.
3:0	RW_O	0x3 0x1 (Device 0 Function 0)	maxlnkspd: This field indicates the maximum link speed of this Port. The encoding is the binary value of the bit location in the Supported Link Speeds Vector in LNKCAP2 that corresponds to the maximum link speed.

6.2.46 lnkcon

PCI Express Link Control

The PCI Express Link Control register controls the PCI Express Link specific parameters. The link control register needs some default values setup by the local host.

Type: CFG **Bus:** 0 **Offset:** 0x1b0 **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0xa0	**PortID:** N/A **Device:** 0 **Device:** 0 **Device:** 2 **Device:** 3		**Function:** 0 (DMI2 Mode) **Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3

Bit	Attr	Default	Description
11:11	RW	0x0	link_autonomous_bandwidth_interrupt_enable: For root ports, when set to 1b this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set.For DMI mode on Dev#0, interrupt is not supported and hence this bit is not useful. Expectation is that BIOS will set bit 27 in MISCCTRLSTS to notify the system of autonomous BW change event on that port.
10:10	RW	0x0	link_bandwidth_management_interrupt_enable: For root ports, when set to 1b this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set.For DMI mode on Dev#0, interrupt is not supported and hence this bit is not useful. Expectation is that BIOS will set bit 27 in MISCCTRLSTS to notify the system of autonomous BW change event on that port.
9:9	RW	0x0	hardware_autonomous_width_disable: When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Note that IIO does not by itself change width for any reason other than reliability. So this bit only disables such a width change as initiated by the device on the other end of the link.
8:8	RO	0x0	enable_clock_power_management:
7:7	RW	0x0	extended_synch: This bit when set forces the transmission of additional ordered sets when exiting L0s and when in recovery.
6:6	RW_V (Function 0) RW (Function 1-3)	0x0	common_clock_configuration: Software sets this bit to indicate that this component and the component at the opposite end of the Link are operating with a common clock source. A value of 0b indicates that this component and the component at the opposite end of the Link are operating with separate reference clock sources. Default value of this bit is 0b. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies in the NFTS. The values used come from these registers depending on the value of this bit: 0: Use NFTS values from CLSPHYCTL3 1: Use NFTS values from CLSPHYCTL4
5:5	WO	0x0	retrain_link: A write of 1 to this bit initiates link retraining in the given PCI Express/DMI port by directing the LTSSM to the recovery state if the current state is [L0, L0s or L1]. If the current state is anything other than L0, L0s, L1 then a write to this bit does nothing. This bit always returns 0 when read.It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.

Type: CFG **Bus:** 0 **Offset:** 0x1b0 **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0xa0	**PortID:** N/A **Device:** 0 **Device:** 0 **Device:** 2 **Device:** 3	**Function:** 0 (DMI2 Mode) **Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
4:4	RW	0x0	link_disable: This field controls whether the link associated with the PCI Express/DMI port is enabled or disabled. When this bit is a 1, a previously configured link would return to the 'disabled' state as defined in the PCI Express Base Specification, Revision 2.0. When this bit is clear, an LTSSM in the 'disabled' state goes back to the detect state. 0: Enables the link associated with the PCI Express port 1: Disables the link associated with the PCI Express port
3:3	RO	0x0	read_completion_boundary: Set to zero to indicate IIO could return read completions at 64B boundaries
1:0	RW_V (Function 0) RW (Function 1-3)	0x0	active_state_link_pm_control: When 01b or 11b, L0s on transmitter is enabled, otherwise it is disabled. 10 and 11 enables L1 ASPM.

6.2.47 lnksts

PCI Express Link Status

The PCI Express Link Status register provides information on the status of the PCI Express Link such as negotiated width, training, and so forth. The link status register needs some default values setup by the local host.

Type: CFG **Bus:** 0 **Offset:** 0x1b2 **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0xa2	**PortID:** N/A **Device:** 0 **Device:** 0 **Device:** 2 **Device:** 3	**Function:** 0 (DMI2 Mode) **Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
15:15	RW1C	0x0	link_autonomous_bandwidth_status: This bit is set to 1b by hardware to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable link operation. IIO does not, on its own, change speed or width autonomously for non-reliability reasons. IIO only sets this bit when it receives a width or speed change indication from downstream component that is not for link reliability reasons.
14:14	RW1C	0x0	link_bandwidth_management_status: This bit is set to 1b by hardware to indicate that either of the following has occurred without the port transitioning through DL_Down status: a) A link retraining initiated by a write of 1b to the Retrain Link bit has completed b) Hardware has autonomously changed link speed or width to attempt to correct unreliable link operation Note IIO also sets this bit when it receives a width or speed change indication from downstream component that is for link reliability reasons.

Type: CFG Bus: 0 Offset: 0x1b2 Bus: 0 Bus: 0 Bus: 0 Offset: 0xa2	PortID: N/A Device: 0 Device: 0 Device: 2 Device: 3	Function: 0 (DMI2 Mode) Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
13:13	RO_V	0x0	data_link_layer_link_active: Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.When this bit is 0b, the transaction layer associated with the link will abort all transactions that would otherwise be routed to that link.
12:12	RW_O	0x1	slot_clock_configuration: This bit indicates whether the processor receives clock from the same xtal that also provides clock to the device on the other end of the link. 1: indicates that same xtal provides clocks to the processor and the slot or device on other end of the link. 0: indicates that different xtals provide clocks to the processor and the slot or device on other end of the link. In general, this field is expected to be set to 1b by BIOS based on board clock routing. This bit has to be set to 1b on DMI mode operation on Device#0.
11:11	RO_V	0x0	link_training: This field indicates the status of an ongoing link training session in the PCI Express port 0: LTSSM has exited the recovery/configuration state. 1: LTSSM is in recovery/configuration state or the Retrain Link was set but training has not yet begun. The IIO hardware clears this bit once LTSSM has exited the recovery/configuration state.
9:4	RO_V	0x0	negotiated_link_width: This field indicates the negotiated width of the given PCI Express link after training is completed. Only x1, x2, x4, x8 and x16 link width negotiations are possible in the processor for Device#1-2 and only x1, x2 and x4 on Device#0. A value of 0x01 in this field corresponds to a link width of x1, 0x02 indicates a link width of x2 and so on, with a value of 0x10 for a link width of x16.The value in this field is reserved and could show any value when the link is not up. Software determines if the link is up or not by reading bit 13 of this register.
3:0	RO_V	0x1	current_link_speed:

6.2.48 sltcap

PCI Express Slot Capabilities

The Slot Capabilities register identifies the PCI Express specific slot capabilities.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xa4	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
31:19	RW_O	0x0	physical_slot_number: This field indicates the physical slot number of the slot connected to the PCI Express port and is initialized by BIOS.
18:18	RO	0x0	command_complete_not_capable: Intel® Xeon® Processor E7 v4 product family is capable of command complete interrupt.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xa4		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
17:17	RW_O	0x0	electromechanical_interlock_present: This bit when set indicates that an Electromechanical Interlock is implemented on the chassis for this slot and that lock is controlled by bit 11 in Slot Control register. This field is initialized by BIOS based on the system architecture.BIOS note: this capability is not set if the Electromechanical Interlock control is connected to main slot power control. This is expected to be used only for Express Module hotpluggable slots.
6:6	RW_O	0x0	hot_plug_capable: This field defines hot-plug support capabilities for the PCI Express port. 0: indicates that this slot is not capable of supporting Hot-plug operations. 1: indicates that this slot is capable of supporting Hot-plug operations This bit is programed by BIOS based on the system design. This bit must be programmed by bios to be consistent with the VPP enable bit for the port.
5:5	RW_O	0x0	hot_plug_surprise: This field indicates that a device in this slot may be removed from the system without prior notification. This field is initialized by BIOS. 0: indicates that hot-plug surprise is not supported 1: indicates that hot-plug surprise is supported Generally this bit is not expected to be set because the only know usage case for this is the ExpressCard FF. But that is not really expected usage in Intel® Xeon® Processor E7 v4 product family context. But this bit is present regardless to allow a usage if it arises. This bit is used by IIO hardware to determine if a transition from DL_active to DL_Inactive is to be treated as a surprise down error or not. If a port is associated with a hotpluggable slot and the hotplug surprise bit is set, then any transition to DLInactive is not considered an error.
4:4	RW_O	0x0	power_indicator_present: This bit indicates that a Power Indicator is implemented for this slot and is electrically controlled by the chassis. 0: indicates that a Power Indicator that is electrically controlled by the chassis is not present 1: indicates that Power Indicator that is electrically controlled by the chassis is present BIOS programs this field with a 1 for CEMExpress Module FFs, if the slot is hotplug capable.
3:3	RW_O	0x0	attention_indicator_present: This bit indicates that an Attention Indicator is implemented for this slot and is electrically controlled by the chassis 0: indicates that an Attention Indicator that is electrically controlled by the chassis is not present 1: indicates that an Attention Indicator that is electrically controlled by the chassis is present BIOS programs this field with a 1 for CEMExpress Module FFs, if the slot is hotplug capable.
2:2	RW_O	0x0	mrl_sensor_present: This bit indicates that an MRL Sensor is implemented on the chassis for this slot. 0: indicates that an MRL Sensor is not present 1: indicates that an MRL Sensor is present BIOS programs this field with a 0 for Express Module FF always. If CEM slot is hotplug capable, BIOS programs this field with either 0 or 1 depending on system design.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xa4	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
1:1	RW_O	0x0	power_controller_present: This bit indicates that a software controllable power controller is implemented on the chassis for this slot. 0: indicates that a software controllable power controller is not present 1: indicates that a software controllable power controller is present BIOS programs this field with a 1 for CEMExpress Module FFs, if the slot is hotplug capable.
0:0	RW_O	0x0	attention_button_present: This bit indicates that the Attention Button event signal is routed from slot or on-board in the chassis to the IIO's hotplug controller. 0: indicates that an Attention Button signal is not routed to IIO 1: indicates that an Attention Button is routed to IIO BIOS programs this field with a 1 for CEMExpress Module FFs, if the slot is hotplug capable.

6.2.49 sltcon

PCI Express Slot Control.

Any write to this register will set the Command Completed bit in the SLTSTS register, only if the VPP enable bit for the port is set. If the port's VPP enable bit is set (i.e. hotplug for that slot is enabled) then the required actions on VPP are completed before the Command Completed bit is set in the SLTSTS register. If the VPP enable bit for the port is clear, then the write simply updates this register see individual bit definitions for details but the Command Completed bit in the SLTSTS register is not set.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xa8	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
12:12	RWS	0x0	data_link_layer_state_changed_enable: When set to 1, this field enables software notification when Data Link Layer Link Active bit in the LNKSTS register changes state
11:11	RW	0x0	electromechanical_interlock_control: When software writes either a 1 to this bit, IIO pulses the EMIL pin per lt;Bluegt;PCI Express ServerWorkstation Module Electromechanical Spec Rev 1.0. Write of 0 has no effect. This bit always returns a 0 when read. If electromechanical lock is not implemented, then either a write of 1 or 0 to this register has no effect.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0xa8		

Bit	Attr	Default	Description
10:10	RWS	0x1	power_controller_control: If a power controller is implemented, when writes to this field will set the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 0: Power On 1: Power Off Note: If the link experiences an unexpected DL_Down condition that is not the result of a Hot Plug removal, the processor follows the PCI Express specification for logging Surprise Link Down. SW is required to set SLTCON[10] to 0 (Power On) in all devices that do not connect to a slot that supports Hot-Plug to enable logging of this error in that device. For devices connected to slots supporting Hot-Plug operations, SLTCON[10] usage to control PWREN# assertion is as described elsewhere.
9:8	RW	0x3	power_indicator_control: If a Power Indicator is implemented, writes to this field will set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00: Reserved. 01: On 10: Blink (IIO drives 1 Hz square wave for Chassis mounted LEDs) 11: Off IIO does not generated the Power_Indicator_On/Off/Blink messages on PCI Express when this field is written to by software.
7:6	RW	0x3	attention_indicator_control: If an Attention Indicator is implemented, writes to this field will set the Attention Indicator to the written state. Reads of this field reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00: Reserved. 01: On 10: Blink (Processor drives 1 Hz square wave) 11: Off IIO does not generated the Attention_Indicator_On/Off/Blink messages on PCI Express when this field is written to by software.
5:5	RW	0x0	hot_plug_interrupt_enable: When set to 1b, this bit enables generation of Hot-Plug interrupt MSI or INTx interrupt depending on the setting of the MSI enable bit in MSICTRL on enabled Hot-Plug events, provided ACPI mode for hotplug is disabled. 0: disables interrupt generation on Hot-plug events 1: enables interrupt generation on Hot-plug events
4:4	RW	0x0	command_completed_interrupt_enable: This field enables software notification Interrupt - MSIINTx or WAKE when a command is completed by the Hot-plug controller connected to the PCI Express port 0 = disables hot-plug interrupts on a command completion by a hot-plug Controller 1 = Enables hot-plug interrupts on a command completion by a hot-plug Controller

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xa8		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
3:3	RW	0x0	presence_detect_changed_enable: This bit enables the generation of hot-plug interrupts or wake messages via a presence detect changed event. 0 = Disables generation of hot-plug interrupts or wake messages when a presence detect changed event happens. 1 = Enables generation of hot-plug interrupts or wake messages when a presence detect changed event happens.
2:2	RW	0x0	mrl_sensor_changed_enable: This bit enables the generation of hot-plug interrupts or wake messages via a MRL Sensor changed event. 0: disables generation of hot-plug interrupts or wake messages when an MRL Sensor changed event happens. 1: Enables generation of hot-plug interrupts or wake messages when an MRL Sensor changed event happens.
1:1	RW	0x0	power_fault_detected_enable: This bit enables the generation of hot-plug interrupts or wake messages via a power fault event. 0 = Disables generation of hot-plug interrupts or wake messages when a power fault event happens. 1 = Enables generation of hot-plug interrupts or wake messages when a power fault event happens.
0:0	RW	0x0	attention_button_pressed_enable: This bit enables the generation of hot-plug interrupts or wake messages via an attention button pressed event. 0 = Disables generation of hot-plug interrupts or wake messages when the attention button is pressed. 1 = Enables generation of hot-plug interrupts or wake messages when the attention button is pressed.

6.2.50 sltsts

PCI Express Slot Status

The PCI Express Slot Status register defines important status information for operations such as hot-plug and Power Management.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xaa		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
8:8	RW1C	0x0	data_link_layer_state_changed: This bit is set (if it is not already set) when the state of the Data Link Layer Link Active bit in the Link Status register changes. Software must read Data Link Layer Active field to determine the link state before initiating configuration cycles to the hot plugged device.
7:7	RO_V	0x0	electromechanical_latch_status: When read this register returns the current state of the Electromechanical Interlock (the EMILS pin) which has the defined encodings as: 0 = Electromechanical Interlock Disengaged 1 = Electromechanical Interlock Engaged

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0xaa		

Bit	Attr	Default	Description
6:6	RO_V	0x0	presence_detect_state: For ports with slots (where the Slot Implemented bit of the PCI Express Capabilities Registers is 1b), this field is the logical OR of the Presence Detect status determined via an in-band mechanism and sideband Present Detect pins. 0 = Card/Module slot empty 1 = Card/module Present in slot (powered or unpowered) For ports with no slots, IIO hardwires this bit to 1b. Note: OS could get confused when it sees an empty PCI Express root port i.e. 'no slots + no presence', since this is now disallowed in the spec. So bios must hide all unused root ports devices in IIO config space, via the DEVHIDE register.
5:5	RO_V	0x0	mrl_sensor_state: This bit reports the status of an MRL sensor if it is implemented. 0 = MRL Closed 1 = MRL Open
4:4	RW1C	0x0	command_completed: This bit is set by IIO when the hot-plug command has completed and the hot-plug controller is ready to accept a subsequent command. It is subsequently cleared by software after the field has been read and processed. This bit provides no guarantee that the action corresponding to the command is complete.Any write to SLTCON (regardless of the port is capable or enabled for hot-plug) is considered a 'hot-plug' command. If the port is not hot-plug capable or hot-plug enabled, then the hot-plug command does not trigger any action on the VPP port but the command is still completed via this bit.
3:3	RW1C	0x0	presence_detect_changed: This bit is set by IIO when the value reported in bit 6 is changes. It is subsequently cleared by software after the field has been read and processed.
2:2	RW1C	0x0	mrl_sensor_changed: This bit is set if the value reported in bit 5 changes. It is subsequently cleared by software after the field has been read and processed.
1:1	RW1C	0x0	power_fault_detected: This bit is set by IIO when a power fault event is detected by the power controller (which is reported via the VPP bit stream). It is subsequently cleared by software after the field has been read and processed.
0:0	RW1C	0x0	attention_button_pressed: This bit is set by IIO when the attention button is pressed. It is subsequently cleared by software after the field has been read and processed. IIO silently discards the AttentionButtonPressed message if received from PCI Express link without updating this bit.

6.2.51 rootcon

PCI Express Root Control.

Type: CFG	**PortID:** N/A	
Bus: 0	**Device:** 0	**Function:** 0
Bus: 0	**Device:** 2	**Function:** 0-3
Bus: 0	**Device:** 3	**Function:** 0-3
Offset: 0xac		

Bit	Attr	Default	Description
4:4	RW	0x0	crsswvisen: CRS software visibility Enable This bit, when set, enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software. If 0, retry status cannot be returned to software.
3:3	RW RW_L (Device 3 Function 0 only)	0x0	pmeinten: This field controls the generation of MSI interrupts INTx interrupts for PME messages. 1 = Enables interrupt generation upon receipt of a PME message 0 = Disables interrupt generation for PME messages
2:2	RW	0x0	sefeen: System Error on Fatal Error Enable This field enables notifying the internal IIO core error logic of occurrence of an uncorrectable fatal error at the port or below its hierarchy. The internal core error logic of IIO then decides if/how to escalate the error further (pins/ message etc). 1: indicates that an internal IIO core error logic notification should be generated if a fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with and including this port. 0: No internal IIO core error logic notification should be generated on a fatal error (ERR_FATAL) reported by any of the devices in the hierarchy associated with and including this port. Note that generation of system notification on a PCI Express fatal error is orthogonal to generation of an MSI/INTx interrupt for the same error. Both a system error and MSI/INTx can be generated on a fatal error or software can chose one of the two. Note that since this register is defined only in PCIe mode for Device#0, this bit will read a 0 in DMI mode. So, to enable core error logic notification on DMI mode fatal errors, BIOS must set bit 35 of MISCCTRLSTS to a 1 (to override this bit) on Device#0 in DMI mode.
1:1	RW	0x0	senfeen: System Error on Non-Fatal Error Enable This field enables notifying the internal IIO core error logic of occurrence of an uncorrectable non-fatal error at the port or below its hierarchy. The internal IIO core error logic then decides if/how to escalate the error further (pins/ message etc). 1: indicates that a internal IIO core error logic notification should be generated if a non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with and including this port. 0: No internal core error logic notification should be generated on a non-fatal error (ERR_NONFATAL) reported by any of the devices in the hierarchy associated with and including this port. Note that generation of system notification on a PCI Express non-fatal error is orthogonal to generation of an MSI/INTx interrupt for the same error. Both a system error and MSI/INTx can be generated on a non-fatal error or software can chose one of the two. Note that since this register is defined only in PCIe mode for Device#0, this bit will read a 0 in DMI mode. So, to enable core error logic notification on DMI mode non-fatal errors, BIOS must set bit 34 of MISCCTRLSTS to a 1 (to override this bit) on Device#0 in DMI mode.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xac	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x0	seceen: System Error on Correctable Error Enable This field controls notifying the internal IIO core error logic of the occurrence of a correctable error in the device or below its hierarchy. The internal core error logic of IIO then decides if/how to escalate the error further (pins/ message etc). 1: indicates that an internal core error logic notification should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with and including this port. 0: No internal core error logic notification should be generated on a correctable error (ERR_COR) reported by any of the devices in the hierarchy associated with and including this port. Note that generation of system notification on a PCI Express correctable error is orthogonal to generation of an MSI/INTx interrupt for the same error. Both a system error and MSI/INTx can be generated on a correctable error or software can chose one of the two. Note that since this register is defined only in PCIe mode for Device#0, this bit will read a 0 in DMI mode. So, to enable core error logic notification on DMI mode correctable errors, BIOS must set bit 33 of MISCCTRLSTS to a 1 (to override this bit) on Device#0 in DMI mode.

6.2.52 rootcap

PCI Express Root Capabilities.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xae	PortID: N/A Device: 0 Device: 2 Device: 3		Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
0:0	RO RW_O (Device 0 Function 0)	0x1 0x0 (Device 0 Function 0, DMI2 mode)	crs_software_visibility: This bit, when set, indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software. Intel® Xeon® Processor E7 v4 product family supports this capability.

6.2.53 rootsts

PCI Express Root Status.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0xb0	**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	 **Function:** 0 (PCIe Mode) **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
17:17	RO_V	0x0	pme_pending: This field indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the pending PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16:16	RW1C	0x0	pme_status: This field indicates a PM_PME message (either from the link or internally from within that root port) was received at the port. 1: PME was asserted by a requester as indicated by the PME Requester ID field This bit is cleared by software by writing a '1'. Note that the root port itself could be the source of a PME event when a hotplug event is observed when the port is in D3hot state.
15:0	RO_V	0x0	pme_requester_id: This field indicates the PCI requester ID of the last PME requestor. If the root port itself was the source of the (virtual) PME message, then a RequesterID of CPUBUSNO0:DevNo:FunctionNo is logged in this field.

6.2.54 devcap2

PCI Express Device Capabilities 2 Register.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 0	**Function:** 0	
Bus: 0	**Device:** 2	**Function:** 0-3	
Bus: 0	**Device:** 3	**Function:** 0-3	
Offset: 0xb4			

Bit	Attr	Default	Description
13:12	RW_O	0x1	tph_completer_supported: Indicates the support for TLP Processing Hints. Processor does not support the extended TPH header. 00: TPH and Extended TPH Completer not supported. 01: TPH Completer supported; Extended TPH Completer not supported. 10: Reserved. 11: Both TPH and Extended TPH Completer supported.
9:9	RO	0x1	atomic128bcascompsup:
8:8	RO	0x1	atomic64bcompsup:
7:7	RO	0x1	atomic32bcompsup:
6:6	RO	0x0	atomicroutsup:
5:5	RW_O	0x1	ari_en: Alternative RID InterpretationCapable This bit is set to 1b indicating Root Port supports this capability.
4:4	RO	0x1	cmpltodissup: Completion Timeout Disable Supported IIO supports disabling completion timeout
3:0	RO	0xe	cmpltovalsup: Completion Timeout Values Supported This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout range. Bits are one-hot encoded and set according to the table below to show timeout value ranges supported. A device that supports the optional capability of Completion Timeout Programmability must set at least two bits.Four time values ranges are defined: Range A: 50 us to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to table below to show timeout value ranges supported. 0000b: Completions Timeout programming not supported – values is fixed by implementation in the range 50 us to 50 ms. 0001b: Range A 0010b: Range B 0011b: Range A & B 0110b: Range B & C 0111b: Range A, B, & C 1110b: Range B, C D 1111b: Range A, B, C & D All other values are reserved. IIO supports timeout values up to 10 ms-64 s

6.2.55 devctrl2

PCI Express Device Control Register 2.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0 (DMI2 Mode)	
Offset: 0xf8			
Bus: 0	Device: 0	Function: 0 (PCIe Mode)	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0xb8			

Bit	Attr	Default	Description
7:7	RO	0x0	atomicegressblock:
6:6	RO	0x0	atomicreqen:
5:5	RW_L	0x0	ari: Alternative RID InterpretationEnable Applies only to root ports. When set to 1b, ARI is enabled for the Root Port. For Device#0 in DMI mode, this bit is ignored
4:4	RW_V (Device 2 and 3 Function 0) RW (Device 0 Function0, Device 2 and 3 Function 1-3)	0x0 0x1 (Device 0 Function 0)	compltodis: Completion Timeout Disable When set to 1b, this bit disables the Completion Timeout mechanism for all NP tx that IIO issues on the PCIe/DMI link. When 0b, completion timeout is enabled. Software can change this field while there is active traffic in the root/ DMI port.
3:0	RW_V (Device 2 and 3 Function 0) RW (Device 0 Function0, Device 2 and 3 Function 1-3)	0x0	compltoval: Completion Timeout Value on NP Tx that IIO issues on PCIe/DMI In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout range. The following encodings and corresponding timeout ranges are defined: 0000b = 10 ms to 50 ms 0001b = Reserved (IIO aliases to 0000b) 0010b = Reserved (IIO aliases to 0000b) 0101b = 16 ms to 55 ms 0110b = 65 ms to 210 ms 1001b = 260 ms to 900 ms 1010b = 1 s to 3.5 s 1101b = 4 s to 13 s 1110b = 17 s to 64 s When software selects 17 s to 64 s range, CTOCTRL further controls the timeout value within that range. For all other ranges selected by OS, the timeout value within that range is fixed in IIO hardware. Software can change this field while there is active traffic in the root port. This value will also be used to control PME_TO_ACK Timeout. That is this field sets the timeout value for receiving a PME_TO_ACK message after a PME_TURN_OFF message has been transmitted. The PME_TO_ACK Timeout has meaning only if bit 6 of MISCCTRLSTS register is set to a 1b.

6.2.56 lnkcap2

PCI Express Link Capabilities 2.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0xbc**				

Bit	Attr	Default	Description
7:1	RW_O	0x7 0x3 (Device 0 Function 0)	lnkspdvec: Supported Link Speeds Vector - This field indicates the supported Link speeds of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions are: Bit 1 2.5 GTs set in CPU Bit 2 5.0 GTs set in CPU Bit 3 8.0 GTs set in CPU Bits 7:4 reserved

6.2.57 lnkcon2

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (DMI2 Mode)**
Offset:	**0x1c0**				
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (PCIe Mode)**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0xc0**				

Bit	Attr	Default	Description
15:12 12:12 (Device 0 Function 0)	RWS	0x0	compliance_de_emphasis: For 8 GT/s Data Rate: This bit sets the Transmitter Preset level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The Encodings are defined as follows: 0000b: -6 dB for de-emphasis, 0 dB for preshoot 0001b: -3.5 dB for de-emphasis, 0 dB for preshoot 0010b: -4.5 dB for de-emphasis, 0 dB for preshoot 0011b: -2.5 dB for de-emphasis, 0 dB for preshoot 0100b: 0 dB for de-emphasis, 0 dB for preshoot 0101b: 0 dB for de-emphasis, 2 dB for preshoot 0110b: 0 dB for de-emphasis, 2.5 dB for preshoot 0111b: -6 dB for de-emphasis, 3.5 dB for preshoot 1000b: -3.5 dB for de-emphasis, 3.5 dB for preshoot 1001b: 0 dB for de-emphasis, 3.5 dB for preshoot Others: reserved For 5 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b: -3.5 dB 0000b: -6 dB For 2.5 GT/s Data Rate: The setting of this field has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this field to 0h. Notes: This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing.
11:11	RWS	0x0	compliance_sos: When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns.

Type: CFG Bus: 0 Offset: 0x1c0 Bus: 0 Bus: 0 Bus: 0 Offset: 0xc0		PortID: N/A Device: 0 Device: 0 Device: 2 Device: 3	Function: 0 (DMI2 Mode) Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
10:10	RWS	0x0	enter_modified_compliance: When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate.
9:7	RWS_V	0x0	transmit_margin: This field controls the value of the nondeemphasized voltage level at the Transmitter pins.
6:6	RW_O	0x0	selectable_de_emphasis: When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component.Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5:5	RWS	0x0	hardware_autonomous_speed_disable: When Set, this bit disables hardware from changing the Link speed for device specific reasons other than attempting to correct unreliable Link operation by reducing Link speed.
4:4	RWS_V	0x0	enter_compliance: Software is permitted to force a link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a link and then initiating a hot reset on the link.
3:0	RWS_V	0x3 0x2 (Device 0 Function 0)	target_link_speed: This field sets an upper limit on link operational speed by restricting the values advertised by the upstream component in its training sequences. Defined encodings are: 0001b 2.5Gb/s Target Link Speed 0010b 5Gb/s Target Link Speed 0011b 8Gb/s Target Link Speed (Reserved for Device 0 Function 0) All other encodings are reserved. If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, IIO will default to Gen1 speed. This field is also used to set the target compliance mode speed when software is using the Enter Compliance bit to force a link into compliance mode.

6.2.58 lnksts2

PCI Express Link Status Register 2.

Type: CFG Bus: 0 Offset: 0x1c2 Bus: 0 Bus: 0 Bus: 0 Offset: 0xc2		PortID: N/A Device: 0 Device: 0 Device: 2 Device: 3	Function: 0 (DMI2 Mode) Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
5:5	RW1CS	0x0	lnkeqreq: This bit is Set by hardware to request Link equalization process to be performed on the link. Reserved for Device 0 Function 0.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (DMI2 Mode)
Offset: 0x1c2		
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0xc2		

Bit	Attr	Default	Description
4:4	RO_V	0x0	eqph3_succ: When set to 1b, this indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed. Reserved for Device 0 Function 0.
3:3	RO_V	0x0	eqph2_succ: When set to 1b, this indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed. Reserved for Device 0 Function 0.
2:2	RO_V	0x0	eqph1_succ: When set to 1b, this indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed. Reserved for Device 0 Function 0.
1:1	RO_V	0x0	eqcmp: When set to 1b, this indicates that the Transmitter Equalization procedure has completed. Reserved for Device 0 Function 0.
0:0	RO_V	0x0	current_de_emphasis_level: When operating at Gen2 speed, this reports the current de-emphasis level. This field is Unused for Gen1 speeds 1b: -3.5 dB 0b: -6 dB

6.2.59 pmcap

Power Management Capabilities

The Power Management Capabilities Register defines the capability ID, next pointer and other power management related support. The following Power Management registers/ capabilities are added for software compliance.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0xe0		

Bit	Attr	Default	Description
31:27	RO_V	0x19	pme_support: For DMI it should be 0, 0x19 for the PCIe ports. Bits 31, 30 and 27 must be set to q1q for PCI-PCI bridge structures representing ports on root complexes.
26:26	RO	0x0	d2_support: Does not support power management state D2.
25:25	RO	0x0	d1_support: Does not support power management state D1.
24:22	RO	0x0	aux_current:
21:21	RO	0x0	device_specific_initialization:

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xe0	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
19:19	RO	0x0	pme_clock: This field is hardwired to 0h as it does not apply to PCI Express.
18:16	RO	0x3	version: This field is set to 3h Power Management 1.2 compliant as version number. Bit is RW-O to make the version 2h incase legacy OS'es have any issues.
15:8	RO	0x0	next_capability_pointer: This is the last capability in the chain and hence set to 0.
7:0	RO	0x1	capability_id: Provides the Power Management capability ID assigned by PCI-SIG.

6.2.60 pmcsr

Power Management Control and Status Register

This register provides status and control information for Power Management events in the PCI Express port of the IIO.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xe4	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
31:24	RO	0x0	data: N/A
23:23	RO	0x0	bus_power_clock_control_enable: N/A
22:22	RO	0x0	b2_b3_support: N/A
15:15	RW1CS	0x0	pme_status: N/A
14:13	RO	0x0	data_scale: N/A
12:9	RO	0x0	data_select: N/A
8:8	RWS RWS_L (Device 3 Function 0)	0x0	pme_enable: N/A
3:3	RW_O	0x1	no_soft_reset: Indicates does not reset its registers when transitioning from D3hot to D0.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0xe4	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
1:0	RW RW_L (Device 0 Function 0)	0x0	power_state: This 2-bit field is used to determine the current power state of the function and to set a new power state as well. 00: D0 01: D1 (not supported by IIO) 10: D2 (not supported by IIO) 11: D3hot If Software tries to write 01 or 10 to this field, the power state does not change from the existing power state which is either D0 or D3hot and nor do these bits1:0 change value. When in D3hot state, IOxAPIC will a) respond to only Type 0 configuration transactions targeted at the device's configuration space, when in D3hot state c) will not respond to memory i.e. D3hot state is equivalent to MSE , accesses to MBAR region note: ABAR region access still go through in D3hot state, if it enabled d) will not generate any MSI writes

6.2.61 xpreut_hdr_ext

REUT PCIe Header Extended.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x100	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
31:20	RO RO_V (Device 0 Function 0)	0x110	pcienextptr: Next Capability Pointer This field contains the offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities. In DMI Mode, it points to the Vendor Specific Error Capability. In PCIe Mode, it points to the ACS Capability.
19:16	RO	0x1	pciecapversion: Capability Version: This field is a PCI-SIG defined version number that indicates the nature and format of the extended capability. This indicates the version of the REUT Capability.
15:0	RO	0xb	pciecapid: PCIe Extended CapID: This field has the value 0Bh to identify the CAP_ID assigned by the PCI SIG indicating a vendor specific capability.

6.2.62 xpreut_hdr_cap

REUT PCIe Header Capability.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x104		

Bit	Attr	Default	Description
31:20	RO	0xc	vseclength: VSEC Length This field defines the length of the REUT ‘capability body’. The size of the leaf body is 12 bytes including the _EXT, _CAP and _LEF registers
19:16	RO	0x0	vsecidrev: REUT VSECID Rev This field is defined as the version number that indicates the nature and format of the VSEC structure. Software must quality the Vendor ID before interpreting this field.
15:0	RO	0x2	vsecid: REUT Engine VSECID This field is an Intel-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field. A value of ‘02h’ is specified for the REUT ‘leaf’ capability structure which resides in each link which in supported by a REUT engine.

6.2.63 xpreut_hdr_lef

REUT Header Leaf Capability.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x108		

Bit	Attr	Default	Description

15:8	RO_V	0x38
		
		0x30 (Device 0 Function 0)
			leafreutdevnum:
			This field identifies the PCI Device/Function # where the REUT engine associated with this link resides.
			Device6 = 00110b & function0 = 000b = 30h

7:0	RO_V	0x7	leafreutengid: This field identifies the REUT engine associated with the link (same as the REUT ID).

6.2.64 acscaphdr

Access Control Services Extended Capability Header.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x110		

Bit	Attr	Default	Description
31:20	RO_V	0x148	next_capability_offset: This field points to the next Capability in extended configuration space. In PCIe Mode, it points to the Advanced Error Capability.
19:16	RO	0x1	capability_version: Set to 1h for this version of the PCI Express logic

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x110		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
15:0	RO	0xd	pci_express_extended_cap_id: Assigned for Access Control Services capability by PCISIG.

6.2.65 acscap

Access Control Services Capability Register.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x114		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
15:8	RO	0x0	egress_control_vector_size: N/A for IIO
6:6	RO	0x0	t: Applies only to root ports. Indicates that the component does not implement ACS Direct Translated P2P.
5:5	RO	0x0	e: Applies only to root portsIndicates that the component does not implement ACS P2P Egress Control.
4:4	RO_V (Device 2 and 3 Function 0) RO (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x1	u: Applies only to root ports. Indicates that the component implements ACS Upstream Forwarding.
3:3	RO_V (Device 2 and 3 Function 0) RO (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x1	c: Applies only to root ports. Indicates that the component implements ACS P2P Completion Redirect.
2:2	RO_V (Device 2 and 3 Function 0) RO (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x1	r: Applies only to root ports. Indicates that the component implements ACS P2P Request Redirect.
1:1	RO_V (Device 2 and 3 Function 0) RO (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x1	b: Applies only to root ports Indicates that the component implements ACS Translation Blocking.
0:0	RO_V (Device 2 and 3 Function 0) RO (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x1	v: Applies only to root ports Indicates that the component implements ACS Source Validation.

6.2.66 acsctrl

Access Control Services Control Register.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (PCIe Mode)
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x116		

Bit	Attr	Default	Description
6:6	RO	0x0	t: Applies only to root ports. This is hardwired to 0b as the component does not implement ACS Direct Translated P2P.
5:5	RO	0x0	e: Applies only to root ports. The component does not implement ACS P2P Egress Control and hence this bit should not be used by SW.
4:4	RW_L (Device 2 and 3 Function 0) RW (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x0	u: When this bit is set, transactions arriving from a root port that target the same port back down, will be forwarded. Normally such traffic would be aborted. Applies only to root ports.
3:3	RW_L (Device 2 and 3 Function 0) RW (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x0	c: Applies only to root ports. Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2:2	RW_L (Device 2 and 3 Function 0) RW (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x0	r: When this bit is set, transactions arriving from a root port that target the same port back down, will be forwarded. Normally such traffic would be aborted. Applies only to root ports.
1:1	RW_L (Device 2 and 3 Function 0) RW (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x0	b: Applies only to root ports. When set, the component blocks all upstream Memory Requests whose Address Translation AT field is not set to the default value.
0:0	RW_L (Device 2 and 3 Function 0) RW (Device 0 Function 0, Device 2 and 3 Function 1-3)	0x0	v: Applies only to root ports. When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary subordinate Bus Numbers.

6.2.67 apicbase

ACPI Base Register.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x140		

Bit	Attr	Default	Description
11:1	RW	0x0	addr: Bits 31:20 are assumed to be 0xFECh. Bits 8:0 are a don't care for address decode. Address decoding to the APIC range is done as APICBASE.ADDR[31:8] <= A[31:8] <= APICLIMIT.ADDR[31:8]. Outbound accesses to the APIC range are claimed by the root port and forwarded to PCIe, if bit 0 is set, even if the MSE bit of the root port is clear or the root port itself is in D3hot state.
0:0	RW	0x0	en: enables the decode of the APIC window

6.2.68 apiclimit

ACPI Limit Register.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x142		

Bit	Attr	Default	Description
11:1	RW	0x0	addr: Applies only to root ports. Bits 31:20 are assumed to be 0xFECh. Bits 8:0 are a don't care for address decode. Address decoding to the APIC range is done as APICBASE.ADDR[31:8] <= A[31:8] <= APICLIMIT.ADDR[31:8]. Outbound accesses to the APIC range are claimed by the root port and forwarded to PCIe, if the range is enabled, even if the MSE bit of the root port is clear or the root port itself is in D3hot state.

6.2.69 vsecphdr

PCI Express Enhanced Capability Header - DMI2 Mode.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0 (DMI2 Mode)
Offset: 0x144		

Bit	Attr	Default	Description
31:20	RO	0x1d0	next_capability_offset: This field points to the next Capability in extended configuration space or is 0 if it is that last capability.
19:16	RO	0x1	capability_version: Set to 1h for this version of the PCI Express logic.

Type: CFG Bus: 0 Offset: 0x144		PortID: N/A Device: 0	Function: 0 (DMI2 Mode)
Bit	**Attr**	**Default**	**Description**
15:0	RO	0xb	pci_express_extended_cap_id: Assigned for Vendor Specific Capability.

6.2.70 vshdr

Vendor Specific Header - DMI2 Mode.

Type: CFG Bus: 0 Offset: 0x148		PortID: N/A Device: 3	Function: 0 (DMI2 Mode)
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x3c	vsec_length: This field points to the next Capability in extended configuration space which is the ACS capability at 150h.
19:16	RO	0x1	vsec_version: Set to 1h for this version of the PCI Express logic
15:0	RO	0x4	vsec_id: Identifies Intel Vendor Specific Capability for AER on DMI

6.2.71 errcaphdr

PCI Express Enhanced Capability Header - Root Ports.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x148		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 (PCIe Mode) Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x1d0	next_capability_offset: This field points to the next Capability in extended configuration space or is 0 if it is that last capability.
19:16	RO	0x1	capability_version: Set to 1h for this version of the PCI Express logic
15:0	RO	0x1	pci_express_extended_cap_id: Assigned for advanced error reporting

6.2.72 uncerrsts

Uncorrectable Error Status.

This register identifies uncorrectable errors detected for PCI Express/DMI port.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 0	**Function:** 0	
Bus: 0	**Device:** 2	**Function:** 0-3	
Bus: 0	**Device:** 3	**Function:** 0-3	
Offset: 0x14c			
Bit	**Attr**	**Default**	**Description**
21:21	RW1CS	0x0	acs_violation_status:
20:20	RW1CS	0x0	received_an_unsupported_request:
19:19	RW1CS	0x0	ecrc_error_status:
18:18	RW1CS	0x0	malformed_tlp_status:
17:17	RW1CS	0x0	receiver_buffer_overflow_status:
16:16	RW1CS	0x0	unexpected_completion_status:
15:15	RW1CS	0x0	completer_abort_status:
14:14	RW1CS	0x0	completion_time_out_status:
13:13	RW1CS	0x0	flow_control_protocol_error_status:
12:12	RW1CS	0x0	poisoned_tlp_status:
5:5	RW1CS	0x0	surprise_down_error_status:
4:4	RW1CS	0x0	data_link_protocol_error_status:

6.2.73 uncerrmsk

Uncorrectable Error Mask.

This register masks uncorrectable errors from being signaled.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 0	**Function:** 0	
Bus: 0	**Device:** 2	**Function:** 0-3	
Bus: 0	**Device:** 3	**Function:** 0-3	
Offset: 0x150			
Bit	**Attr**	**Default**	**Description**
21:21	RWS	0x0	acs_violation_mask:
20:20	RWS	0x0	unsupported_request_error_mask:
19:19	RWS	0x0	ecrc_error_mask:
18:18	RWS	0x0	malformed_tlp_mask:
17:17	RWS	0x0	receiver_buffer_overflow_mask:
16:16	RWS	0x0	unexpected_completion_mask:
15:15	RWS	0x0	completer_abort_mask:
14:14	RWS	0x0	completion_time_out_mask:
13:13	RWS	0x0	flow_control_protocol_error_mask:
12:12	RWS	0x0	poisoned_tlp_mask:
5:5	RWS	0x0	surprise_down_error_mask:
4:4	RWS	0x0	data_link_layer_protocol_error_mask:

6.2.74 uncerrsev

Uncorrectable Error Severity.

This register indicates the severity of the uncorrectable errors.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x154**				

Bit	Attr	Default	Description
21:21	RWS	0x0	acs_violation_severity:
20:20	RWS	0x0	unsupported_request_error_severity:
19:19	RWS	0x0	ecrc_error_severity:
18:18	RWS	0x1	malformed_tlp_severity:
17:17	RWS	0x1	receiver_buffer_overflow_severity:
16:16	RWS	0x0	unexpected_completion_severity:
15:15	RWS	0x0	completer_abort_severity:
14:14	RWS	0x0	completion_time_out_severity:
13:13	RWS	0x1	flow_control_protocol_error_severity:
12:12	RWS	0x0	poisoned_tlp_severity:
5:5	RWS	0x1	surprise_down_error_severity:
4:4	RWS	0x1	data_link_protocol_error_severity:

6.2.75 corerrsts

Correctable Error Status.

This register identifies the status of the correctable errors that have been detected by the PCI Express port.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x158**				

Bit	Attr	Default	Description
13:13	RW1CS	0x0	advisory_non_fatal_error_status:
12:12	RW1CS	0x0	replay_timer_time_out_status:
8:8	RW1CS	0x0	replay_num_rollover_status:
7:7	RW1CS	0x0	bad_dllp_status:
6:6	RW1CS	0x0	bad_tlp_status:
0:0	RW1CS	0x0	receiver_error_status:

6.2.76 corerrmsk

Correctable Error Mask.

This register masks correctable errors from being signaled.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x15c		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
13:13	RWS	0x1	advisory_non_fatal_error_mask:
12:12	RWS	0x0	replay_timer_time_out_mask:
8:8	RWS	0x0	replay_num_rollover_mask:
7:7	RWS	0x0	bad_dllp_mask:
6:6	RWS	0x0	bad_tlp_mask:
0:0	RWS	0x0	receiver_error_mask:

6.2.77 errcap

Advanced Error capabilities and Control Register.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x160		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
8:8	RWS	0x0	ecrc_check_enable: PCIe ECRC enable.
7:7	RW_O	0x1	ecrc_check_capable: PCIe ECRC capable.
6:6	RWS	0x0	ecrc_generation_enable: PCIe ECRC generation enable.
5:5	RW_O	0x1	ecrc_generation_capable: PCIe ECRC generation capable.
4:0	ROS_V	0x0	first_error_pointer: The First Error Pointer is a read-only register that identifies the bit position of the first unmasked error reported in the Uncorrectable Error register. In case of two errors happening at the same time, fatal error gets precedence over non-fatal, in terms of being reported as first error. This field is rearmed to capture new errors when the status bit indicated by this field is cleared by software.

6.2.78 hdrlog[0:3]

Header Log 0-3.

This register contains the header log when the first error occurs. Headers of the subsequent errors are not logged.

Type: CFG		PortID: N/A	
Bus: 0		Device: 0	Function: 0
Bus: 0		Device: 2	Function: 0-3
Bus: 0		Device: 3	Function: 0-3
Offset: 0x164, 0x168, 0x16c, 0x170			

Bit	Attr	Default	Description
31:0	ROS_V	0x0	hdr: Logs the first DWORD of the header on an error condition.

6.2.79 rperrcmd

Root Port Error Command.

This register controls behavior upon detection of errors.

Type: CFG		PortID: N/A	
Bus: 0		Device: 0	Function: 0
Bus: 0		Device: 2	Function: 0-3
Bus: 0		Device: 3	Function: 0-3
Offset: 0x174			

Bit	Attr	Default	Description
2:2	RW	0x0	fatal_error_reporting_enable: Applies to root ports onlyEnable MSI INTx interrupt on fatal errors when set.
1:1	RW	0x0	non_fatal_error_reporting_enable: Applies to root ports onlyEnable interrupt on a non-fatal error when set.
0:0	RW	0x0	correctable_error_reporting_enable: Applies to root ports onlyEnable interrupt on correctable errors when set.

6.2.80 rperrsts

Root Port Error Status.

The Root Error Status register reports status of error Messages (ERR_COR), ERR_NONFATAL, and ERR_FATAL) received by the Root Complex in IIO, and errors detected by the Root Port itself (which are treated conceptually as if the Root Port had sent an error Message to itself). The ERR_NONFATAL and ERR_FATAL Messages are grouped together as uncorrectable. Each correctable and uncorrectable (Non-fatal and Fatal) error source has a first error bit and a next error bit associated with it respectively. When an error is received by a Root Complex, the respective first error bit is set and the Requestor ID is logged in the Error Source Identification register. A set individual error status bit indicates that a particular error category occurred; software may clear an error status by writing a 1 to the respective bit. If software does not clear the first reported error before another error Message is received of the same category (correctable or uncorrectable), the corresponding next error status bit will be set but the Requestor ID of the subsequent error Message is discarded. The next error status bits may be cleared by software by writing a 1 to the respective bit as well.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x178		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
31:27	RO	0x0	advanced_error_interrupt_message_number: Advanced Error Interrupt Message Number offset between base message data an the MSI message if assigned more than one message number. IIO hardware automatically updates this register to 0x1h if the number of messages allocated to the root port is 2.
6:6	RW1CS	0x0	fatal_error_messages_received: Set when one or more Fatal Uncorrectable error Messages have been received.
5:5	RW1CS	0x0	non_fatal_error_messages_received: Set when one or more Non-Fatal Uncorrectable error Messages have been received.
4:4	RW1CS	0x0	first_uncorrectable_fatal: Set when bit 2 is set (from being clear) and the message causing bit 2 to be set is an ERR_FATAL message.
3:3	RW1CS	0x0	multiple_error_fatal_nonfatal_received: Set when either a fatal or a non-fatal error message is received and Error Fatal/Nonfatal Received is already set, that is, log from the 2nd Fatal or No fatal error message onwards.
2:2	RW1CS	0x0	error_fatal_nonfatal_received: Set when either a fatal or a non-fatal error message is received and this bit is already not set. i.e. log the first error message. Note that when this bit is set bit 3 could be either set or clear.
1:1	RW1CS	0x0	multiple_correctable_error_received: Set when either a correctable error message is received and Correctable Error Received bit is already set, that is, log from the 2nd Correctable error message onwards .
0:0	RW1CS	0x0	correctable_error_received: Set when a correctable error message is received and this bit is already not set, that is, log the first error message.

6.2.81 errsid

Error Source Identification.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x17c		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
31:16	ROS_V	0x0	fatal_non_fatal_error_source_id: Requestor ID of the source when an Fatal or Non Fatal error message is received and the Error Fatal/Nonfatal Received bit is not already set, that is, log ID of the first Fatal or Non Fatal error message. Note that when the root port itself is the cause of the received message (virtual message), then a Source ID of CPUBUSNO0:DevNo:0 is logged into this register.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x17c			

Bit	Attr	Default	Description
15:0	ROS_V	0x0	correctable_error_source_id: Requestor ID of the source when a correctable error message is received and the Correctable Error Received bit is not already set, that is, log ID of the first correctable error message. Note that when the root port itself is the cause of the received message (virtual message), then a Source ID of CPUBUSNO0:DevNo:0 is logged into this register.

6.2.82 perfctrlsts_0

Performance Control and Status Register 0.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x180			

Bit	Attr	Default	Description
20:16	RW	0x18	outstanding_requests_gen1:
13:8	RW	0x30	outstanding_requests_gen2:
7:7	RW	0x1	use_allocating_flow_wr: Use Allocating Flows for 'Normal Writes' on VC0 and VCp 1: Use allocating flows for the writes that meet the following criteria. 0: Use non-allocating flows for writes that meet the following criteria. (TPH=0 OR TPHDIS=1 OR (TPH=1 AND Tag=0 AND CIPCTRL[28]=1)) AND (NS=0 OR NoSnoopOpWrEn=0) AND Non-DCA Write Note: VC1/VCm traffic is not impacted by this bit in Dev#0 When allocating flows are used for the above write types, IIO does not send a Prefetch Hint message. Current recommendation for BIOS is to just leave this bit at default of 1b for all but DMI port. For DMI port when operating in DMI mode, this bit must be left at default value and when operating in PCIe mode, this bit should be set by BIOS. Note there is a coupling between the usage of this bit and bits 2 and 3. TPHDIS is bit 0 of this register NoSnoopOpWrEn is bit 3 of this register
6:6	RW	0x0	vcp_nosnoopopen: Enables inbound VCp traffic with NS=1 to issue non-snoop IDI/QPI requests.
5:5	RW	0x0	vc1m_nosnoopopdis — Disables inbound VC1/m traffic with NS=1 from issuing nonsnoop IDI/QPI requests.
4:4	RW	0x1	read_stream_interleave_size:

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x180	**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	 **Function:** 0 **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
3:3	RW	0x0	nosnoopopwren: Enable No-Snoop Optimization on VC0 writes and VCp writes This applies to writes with the following conditions: NS=1 AND (TPH=0 OR TPHDIS=1) 1: Inbound writes to memory with above conditions will be treated as non-coherent (no snoops) writes on Intel QPI 0: Inbound writes to memory with above conditions will be treated as allocating or non-allocating writes, depending on bit 4 in this register. If TPH=1 and TPHDIS=0 then NS is ignored and this bit is ignored VC1/VCm writes are not controlled by this bit since they are always non-snoop and can be no other way. Current recommendation for BIOS is to just leave this bit at default of 0b.
2:2	RW	0x0	nosnoopoprden: Enable No-Snoop Optimization on VC0 reads and VCp reads This applies to reads with the following conditions: NS=1 AND (TPH=0 OR TPHDIS=1) 1: When the condition is true for a given inbound read request to memory, it will be treated as non-coherent (no snoops) reads on Intel QPI. 0: When the condition is true for a given inbound read request to memory, it will be treated as normal snooped reads from PCIe (which trigger a PCIRdCurrent or DRd.UC on IDI). Notes: If TPH=1 and TPHDIS=0 then NS is ignored and this bit is ignored VC1 and VCm reads are not controlled by this bit and those reads are always non-snoop. Current recommendation for BIOS is to just leave this bit at default of 0b.
1:1	RW	0x0	read_passing_read_disable: Disable reads bypassing other reads.
0:0	RW	0x1	read_stream_policy:

6.2.83 perfctrlsts_1

Performance Control and Status Register 1.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x184	**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	 **Function:** 0 **Function:** 0-3 **Function:** 0-3	
Bit	**Attr**	**Default**	**Description**
9:9	RW	0x0	tphdis: TLP Processing Hint Disable When set, writes or reads with TPH=1, will be treated as if TPH=0.
8:8	RW	0x0	dca_reqid_override: DCA Requester ID Override When this bit is set, Requester ID match for DCA writes is bypassed. All writes from the port are treated as DCA writes and the tag field will convey if DCA is enabled or not and the target information.
3:3	RW	0x0	max_read_completion_combine_size:

6.2.84 miscctrlsts_0

MISC Control and Status Register 0.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x188			

Bit	Attr	Default	Description
31:31	RW	0x0	disable_l0s_on_transmitter: When set, IIO never puts its tx in L0s state, even if OS enables it via the Link Control register.
30:30	RW_O	0x1	inbound_io_disable:
29:29	RW	0x1	cfg_to_en: Disables/enables config timeouts, independently of other timeouts.
28:28	RW	0x0	to_dis: Disables timeouts completely.
27:27	RWS	0x0	system_interrupt_only_on_link_bw_management_status: This bit, when set, will disable generating MSI and Intx interrupts on link bandwidth (speed and/or width) and management changes, even if MSI or INTx is enabled i.e. will disable generating MSI or INTx when LNKSTS bits 15 and 14 are set. Whether or not this condition results in a system event like Intel SMI/PMI/CPEI is dependent on whether this event masked or not in the XPCORERRMSK register.
24:24	RW	0x0	peer2peer_memory_read_disable: When set, peer-to-peer memory reads are master aborted otherwise they are allowed to progress per the peer-to-peer decoding rules.
23:23	RW	0x0	phold_disable: Applies only to Dev#0When set, the IIO responds with Unsupported request on receiving assert_phold message from PCH and results in generating a fatal error.
22:22	RWS	0x0	check_cpl_tc:
21:21	RW_O	0x0	zero_ob_tc: Forces the TC field to zero for outbound requests. 1: TC is forced to zero on all outbound transactions regardless of the source TC value 0: TC is not altered ***Note***: In DMI mode, TC is always forced to zero and this bit has no effect.
20:20	RW	0x1	maltlp_32baddr64bhdr_en: When set, enables reporting a Malformed packet when the TLP is a 32 bit address in a 4DW header. PCI Express forbids using 4DW header sizes when the address is less than 4 GB, but some cards may use the 4DW header anyway. In these cases, the upper 32 bits of address are all 0.
18:18	RWS	0x0	max_read_completion_combine_size: When set, all completions are returned without combining. Completions are naturally broken on cacheline boundaries, so all completions will be 64B or less.
17:17	RO	0x0	force_data_perr: Force Data Parity Error.
16:16	RO	0x0	force_ep_biterr: Force EP Bit Error (Poison Bit).

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0**
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x188**				

Bit	Attr	Default	Description
15:15	RWS	0x0	dis_hdr_storage:
14:14	RWS	0x0	allow_one_np_os:
13:13	RWS	0x0	tlp_on_any_lane:
12:12	RWS	0x1	disable_ob_parity_check:
11:11	RWS	0x1	allow_1nonvc1_after_10vc1s: Allow a non-VC1 request from DMI to go after every ten VC1 request (to prevent starvation of non-VC1). Only available for Device 0 Function 0.
9:9	RWS	0x0	dispdspolling: Disables gen2 if timeout happens in polling.cfg.
8:7	RW	0x0	pme2acktoctrl:
6:6	RW	0x0	enable_timeout_for_receiving_pme_to_ack: When set, IIO enables the timeout to receiving the PME_TO_ACK
5:5	RW_V	0x0	send_pme_turn_off_message: When this bit is written with a 1b, IIO sends a PME_TURN_OFF message to the PCIe link. Hardware clears this bit when the message has been sent on the link.
4:4	RW	0x0	enable_system_error_only_for_aer: Applies only to root ports. For Dev#0 in DMI mode, this bit is to be left at default value always.When this bit is set, the PCI Express errors do not trigger an MSI or Intx interrupt, regardless of the whether MSI or INTx is enabled or not. Whether or not PCI Express errors result in a system event like NMI/Intel SMI/PMI/CPEI is dependent on whether the appropriate system error or override system error enable bits are set or not. When this bit is clear, PCI Express errors are reported via MSI or INTx and/or NMI/Intel SMI/MCA/CPEI. When this bit is clear, and ‘System Error on Fatal Error Enable’ bit in ROOTCON register is set, then NMI/Intel SMI/MCA is (also) generated for a PCI Express fatal error. Similar behavior for non-fatal and corrected errors.
3:3	RW	0x0	enable_acpi_mode_for_hotplug: Applies only to root ports. For Dev#0 in DMI mode, this bit is to be left at default value always. When this bit is set, all hotplug events from the PCI Express port are handled via _HPGPE messages to the PCH and no MSI/INTx messages are ever generated for hotplug events (regardless of whether MSI or INTx is enabled at the root port or not) at the root port. When this bit is clear, _HPGPE message generation on behalf of root port hotplug events is disabled and OS can chose to generate MSI or INTx interrupt for hotplug events, by setting the MSI enable bit in root ports

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x188	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
2:2	RW	0x0	enable_acpi_mode_for_pm: Applies only to root ports. For Dev#0 in DMI mode, this bit is to be left at default value always. When this bit is set, all Power Management events at the PCI Express port are handled via _PMEGPE messages to the PCH, and no MSI interrupts are ever generated for Power Management events at the root port (regardless of whether MSI is enabled at the root port or not). When clear, _PMEGPE message generation for Power Management events is disabled and OS can chose to generate MSI interrupts for delivering Power Management events by setting the MSI enable bit in root ports.
1:1	RW_O	0x0	inbound_configuration_enable: Enable Inbound Configuration Requests.

6.2.85 miscctrlsts_1

MISC Control and Status Register 1.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x18c	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
19:19	RW	0x1	vcm_arb_in_vc1: Only available for Device 0 Function 0.
18:18	RW	0x0	no_vcm_throttle_in_quiesce: Only available for Device 0 Function 0
17:17	RW1CS	0x0	locked_read_timed_out: Indicates that a locked read request incurred a completion time-out on PCI Express/DMI
16:16	RW1C	0x0	received_pme_to_ack: Indicates that IIO received a PME turn off ack packet or it timed out waiting for the packet
9:9	RW	0x0	override_socketid_in_cplid: For TPH/DCA requests, the Completer ID can be returned with SocketID when this bit is set.
6:6	RW	0x0	problematic_port_for_lock_flows: This bit is set by BIOS when it knows that this port is connected to a device that creates Posted-Posted dependency on its In-Out queues. This bit is set on a link if: IIO lock flows depend on the setting of this bit to treat this port in a special way during the flows. Note that if BIOS is setting up the lock flow to be in the ' Intel QPI compatible' mode, then this bit must be set to 0. Notes: An inbound MSI request can block the posted channel until EOI's are posted to all outbound queues enabled to receive EOI. Because of this, this bit cannot be set unless EOIFD is also set.

Type: CFG **Bus:** 0 **Bus:** 0 **Bus:** 0 **Offset:** 0x18c		**PortID:** N/A **Device:** 0 **Device:** 2 **Device:** 3	**Function:** 0 **Function:** 0-3 **Function:** 0-3
Bit	**Attr**	**Default**	**Description**
4:4	RWS	0x0	formfactor: Indicates what form-factor a particular root port controls 0 - CEM 1 - Express Module This bit is used to interpret bit 6 in the VPP serial stream for the port as either MRL# (CEM) input or EMLSTS# (Express Module) input.
3:3	RW	0x0	override_system_error_on_pcie_fatal_error_enable: When set, fatal errors on PCI Express (that have been successfully propagated to the primary interface of the port) are sent to the IIO core error logic (for further escalation) regardless of the setting of the equivalent bit in the ROOTCTRL register. When clear, the fatal errors are only propagated to the IIO core error logic if the equivalent bit in ROOTCTRL register is set. For Dev#0 in DMI mode and Dev#3/Fn#0, unless this bit is set, DMI link related fatal errors will never be notified to system software.
2:2	RW	0x0	override_system_error_on_pcie_non_fatal_error_enable: When set, non-fatal errors on PCI Express (that have been successfully propagated to the primary interface of the port) are sent to the IIO core error logic (for further escalation) regardless of the setting of the equivalent bit in the ROOTCTRL register. When clear, the non-fatal errors are only propagated to the IIO core error logic if the equivalent bit in ROOTCTRL register is set. For Dev#0 in DMI mode and Dev#3/Fn#0, unless this bit is set, DMI link related non-fatal errors will never be notified to system software.
1:1	RW	0x0	override_system_error_on_pcie_correctable_error_enable: When set, correctable errors on PCI Express (that have been successfully propagated to the primary interface of the port) are sent to the IIO core error logic (for further escalation) regardless of the setting of the equivalent bit in the ROOTCTRL register. When clear, the correctable errors are only propagated to the IIO core error logic if the equivalent bit in ROOTCTRL register is set. For Dev#0 in DMI mode and Dev#3/Fn#0, unless this bit is set, DMI link related correctable errors will never be notified to system software.
0:0	RW	0x0	acpi_pme_inten: When set, Assert/Deassert_PMEGPE messages are enabled to be generated when ACPI mode is enabled for handling PME messages from PCI Express. When this bit is cleared (from a 1), a Deassert_PMEGPE message is scheduled on behalf of the root port if an Assert_PMEGPE message was sent last from the root port.

6.2.86 pcie_iou_bif_ctrl

PCIe Port Bifurcation Control.

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0**
Bus:	**0**	**Device:**	**2**	**Function:**	**0**
Bus:	**0**	**Device:**	**3**	**Function:**	**0**
Offset:	**0x190**				

Bit	Attr	Default	Description
3:3	WO	0x0	iou_start_bifurcation: When software writes a 1 to this bit, IIO starts the port 0 bifurcation process. After writing to this bit, software can poll the Data Link Layer link active bit in the LNKSTS register to determine if a port is up and running. Once a port bifurcation has been initiated by writing a 1 to this bit, software cannot initiate any more write-1 to this bit (write of 0 is ok). Notes: That this bit can be written to a 1 in the same write that changes values for bits 2:0 in this register and in that case, the new value from the write to bits 2:0 take effect. This bit always reads a 0b.
2:0	RWS RO (Device 0 Function 0)	0x4 0x0 (Device 0 Function 0)	iou_bifurcation_control: To select a IOU bifurcation, software sets this field and then either a) sets bit 3 in this register to initiate training OR b) resets the entire Intel® Xeon® Processor E7 v4 product family and on exit from that reset, CPU will bifurcate the ports per the setting in this field. For Device 1 Function 0: 000: x4x4 (operate lanes 7:4 as x4, 3:0 as x4) 001: x8 For Device 2 and Device 3 Function 0: 000: x4x4x4x4 operate lanes 15:12 as x4, 11:8 as x4, 7:4 as x4 and 3:0 as x4 001: x4x4x8 operate lanes 15:12 as x4, 11:8 as x4 and 7:0 as x8 010: x8x4x4 operate lanes 15:8 as x8, 7:4 as x4 and 3:0 as x4 011: x8x8 operate lanes 15:8 as x8, 7:0 as x8 100: x16 others: Reserved For Device 0 Function 0, read only.

6.2.87 dmictrl

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**0**	**Function:**	**0 (DMI2 Mode)**
Offset:	**0x1a0**				

Bit	Attr	Default	Description
0:0	RW	0x1	Setting this bit causes IIO to abort all inbound requests on the DMI port. This will be used during specific power state and reset transitions to prevent request from PCH. This bit does not apply in PCI Express mode. Inbound posted requests will be dropped and inbound non-posted requests will be completed with Unsupported Request completion. Completions flowing inbound (from outbound requests) will not be dropped, but will be forwarded normally. This bit will not affect S-state auto-completion, if it is enabled.

6.2.88 dmists

Type: CFG Bus: 0 Offset: 0x1a8	PortID: N/A Device: 0	Function: 0 (DMI2 Mode)	
Bit	**Attr**	**Default**	**Description**
0:0	RW1C	0x0	received_cpu_reset_done_ack:

6.2.89 ERRINJCAP

PCI Express Error Injection Capability.

Defines a vendor specific capability for WHEA error injection.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x1d0	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x250 0x280 (Device 0 Function 0)	nxtptr: Next Capability Offset This field points to the next capability or 0 if there isn't a next capability.
19:16	RO	0x1	capver: Capability Version Set to 2h for this version of the PCI Express specification
15:0	RO	0xb	extcapid: PCI Express Extended Capability ID Vendor Defined Capability

6.2.90 ERRINJHDR

PCI Express Error Injection Capability Header.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x1d4	PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
31:20	RO	0xa	vseclen: Vendor Specific Capability Length Indicates the length of the capability structure, including header bytes.
19:16	RO	0x1	vsecrev: Vendor Specific Capability Revision Set to 1h for this version of the WHEA Error Injection logic.
15:0	RO	0x3	vsecid: Vendor Specific ID Assigned for WHEA Error Injection

6.2.91 ERRINJCON

PCI Express Error Injection Control Register.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 0	**Function:** 0	
Bus: 0	**Device:** 2	**Function:** 0-3	
Bus: 0	**Device:** 3	**Function:** 0-3	
Offset: 0x1d8			

Bit	Attr	Default	Description
2:2	RW	0x0	cause_ctoerr: Cause a Completion Timeout Error When this bit is written to transition from 0 to 1, one and only one error assertion pulse is produced on the error source signal for the given port. This error will appear equivalent to an actual error assertion because this event is OR'd into the existing error reporting structure. To log another error, this bit must be cleared first, before setting again. Leaving this bit in a 1 state does not produce a persistent error condition. ***Notes:*** This bit is used for an uncorrectable error test This bit must be cleared by software before creating another event. This bit is disabled by bit 0 of this register
1:1	RW	0x0	cause_rcverr: Cause a Receiver Error When this bit is written to transition from 0 to 1, one and only one error assertion pulse is produced on the error source signal for the given port. This error will appear equivalent to an actual error assertion because this event is OR'd into the existing error reporting structure. To log another error, this bit must be cleared first, before setting again. Leaving this bit in a 1 state does not produce a persistent error condition. ***Notes:*** This bit is used for an correctable error test This bit must be cleared by software before creating another event. This bit is disabled by bit 0 of this register
0:0	RW_O	0x0	errinjdis: Error Injection Disable This bit disables the use of the PCIe error injection bits.

6.2.92 ctoctrl

Completion Timeout Control.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 0	**Function:** 0	
Bus: 0	**Device:** 2	**Function:** 0-3	
Bus: 0	**Device:** 3	**Function:** 0-3	
Offset: 0x1e0			

Bit	Attr	Default	Description
9:8	RW	0x0	xp_to_pcie_timeout_select: When OS selects a timeout range of 17s to 64s for XP (that affect NP tx issued to the PCIe/DMI) using the root port's DEVCTRL2 register, this field selects the sub-range within that larger range, for additional controllability. 00 : 17s-30s 01 : 31s-45s 10 : 46s-64s 11 : Reserved

6.2.93 xpcorerrsts

XP Correctable Error Status

The architecture model for error logging and escalation of internal errors is similar to that of PCI Express AER, except that these internal errors never trigger an MSI and are always reported to the system software. Mask bits mask the reporting of an error and severity bit controls escalation to either fatal or non-fatal error to the internal core error logic. Note that internal errors detected in the PCI Express cluster are not dependent on any other control bits for error escalation other than the mask bit defined in these registers. All these registers are sticky.

Type: CFG **Bus: 0** **Bus: 0** **Bus: 0** **Offset: 0x200**	**PortID: N/A** **Device: 0** **Device: 2** **Device: 3**	**Function: 0** **Function: 0-3** **Function: 0-3**	
Bit	**Attr**	**Default**	**Description**
1:1	RW1CS	0x0	msgd_gt_16dw: This bit is set if the root port receives a message with greater than 16 dwords (64 bytes of data).
0:0	RW1CS	0x0	pci_link_bandwidth_changed_status: This bit is set when the logical OR of LNKSTS[15] and LNKSTS[14] goes from 0 to 1.

6.2.94 xpcorerrmsk

XP Correctable Error Mask.

Type: CFG **Bus: 0** **Bus: 0** **Bus: 0** **Offset: 0x204**	**PortID: N/A** **Device: 0** **Device: 2** **Device: 3**	**Function: 0** **Function: 0-3** **Function: 0-3**	
Bit	**Attr**	**Default**	**Description**
0:0	RWS	0x0	pci_link_bandwidth_changed_mask: Masks the BW change event from being propagated to the IIO core error logic as a correctable error

6.2.95 xpuncerrsts

XP Uncorrectable Error Status.

Type: CFG **Bus: 0** **Bus: 0** **Bus: 0** **Offset: 0x208**	**PortID: N/A** **Device: 0** **Device: 2** **Device: 3**	**Function: 0** **Function: 0-3** **Function: 0-3**	
Bit	**Attr**	**Default**	**Description**
9:9	RW1CS	0x0	outbound_poisoned_data: Set when outbound poisoned data (from Intel QPI or peer, write or read completion) is received by this port
8:8	RW1CS	0x0	received_msi_writes_greater_than_a_dword_data:

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x208	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
6:6	RW1CS	0x0	received_pcie_completion_with_ur_status:
5:5	RW1CS	0x0	received_pcie_completion_with_ca_status:
4:4	RW1CS	0x0	sent_completion_with_unsupported_request:
3:3	RW1CS	0x0	sent_completion_with_completer_abort:
1:1	RW1CS	0x0	outbound_switch_fifo_data_parity_error_detected:

6.2.96 xpuncerrmsk

XP Uncorrectable Error Mask.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x20c	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
9:9	RWS	0x0	outbound_poisoned_data_mask: Masks signaling of stop and scream condition to the core error logic.
8:8	RWS	0x0	received_msi_writes_greater_than_a_dword_data_mask:
6:6	RWS	0x0	received_pcie_completion_with_ur_status_mask:
5:5	RWS	0x0	received_pcie_completion_with_ca_status_mask:
4:4	RWS	0x0	sent_completion_with_unsupported_request_mask:
3:3	RWS	0x0	sent_completion_with_completer_abort_mask:
1:1	RWS	0x0	outbound_switch_fifo_data_parity_error_detected_mask:

6.2.97 xpuncerrsev

XP Uncorrectable Error Severity

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x210	PortID: N/A Device: 0 Device: 2 Device: 3	 Function: 0 Function: 0-3 Function: 0-3	
Bit	**Attr**	**Default**	**Description**
9:9	RWS	0x0	outbound_poisoned_data_severity:
8:8	RWS	0x0	received_msi_writes_greater_than_a_dword_data_severity:
6:6	RWS	0x0	received_pcie_completion_with_ur_status_severity:
5:5	RWS	0x0	received_pcie_completion_with_ca_status_severity:
4:4	RWS	0x0	sent_completion_with_unsupported_request_severity:
3:3	RWS	0x0	sent_completion_with_completer_abort_severity:
1:1	RWS	0x1	outbound_switch_fifo_data_parity_error_detected_severity:

6.2.98 xpuncerrptr

XP Uncorrectable Error Pointer.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x214			

Bit	Attr	Default	Description
4:0	ROS_V	0x0	xp_uncorrectable_first_error_pointer: This field points to which of the unmasked uncorrectable errors happened first. This field is only valid when the corresponding error is unmasked and the status bit is set and this field is rearmed to load again when the status bit indicated to by this pointer is cleared by software from 1 to 0. Value of 0x0 corresponds to bit 0 in XPUNCERRSTS register, value of 0x1 corresponds to bit 1 and so forth.

6.2.99 uncedmask

Uncorrectable Error Detect Status Mask

This register masks PCIe link related uncorrectable errors from causing the associated AER status bit to be set.

Type: CFG	PortID: N/A		
Bus: 0	Device: 0	Function: 0	
Bus: 0	Device: 2	Function: 0-3	
Bus: 0	Device: 3	Function: 0-3	
Offset: 0x218			

Bit	Attr	Default	Description
21:21	RWS	0x0	acs_violation_detect_mask:
20:20	RWS	0x0	received_an_unsupported_request_detect_mask:
19:19	RWS	0x0	ecrc_error_detect_mask:
18:18	RWS	0x0	malformed_tlp_detect_mask:
17:17	RWS	0x0	receiver_buffer_overflow_detect_mask:
16:16	RWS	0x0	unexpected_completion_detect_mask:
15:15	RWS	0x0	completer_abort_detect_mask:
14:14	RWS	0x0	completion_time_out_detect_mask:
13:13	RWS	0x0	flow_control_protocol_error_detect_mask:
12:12	RWS	0x0	poisoned_tlp_detect_mask:
5:5	RWS	0x0	surprise_down_error_detect_mask:
4:4	RWS	0x0	data_link_layer_protocol_error_detect_mask:

6.2.100 coredmask

Correctable Error Detect Status Mask

This register masks PCIe link related correctable errors from causing the associated status bit in AER status register to be set.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x21c		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
13:13	RWS	0x0	advisory_non_fatal_error_detect_mask:
12:12	RWS	0x0	replay_timer_time_out_detect_mask:
8:8	RWS	0x0	replay_num_rollover_detect_mask:
7:7	RWS	0x0	bad_dllp_detect_mask:
6:6	RWS	0x0	bad_tlp_detect_mask:
0:0	RWS	0x0	receiver_error_detect_mask:

6.2.101 rpedmask

Root Port Error Detect Status Mask

This register masks the associated error messages (received from PCIe link and NOT the virtual ones generated internally), from causing the associated status bits in AER to be set.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x220		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
2:2	RWS	0x0	fatal_error_detected_status_mask:
1:1	RWS	0x0	non_fatal_error_detected_status_mask:
0:0	RWS	0x0	correctable_error_detected_status_mask:

6.2.102 xpuncedmask

XP Uncorrectable Error Detect Mask

This register masks other uncorrectable errors from causing the associated XPUNCERRSTS status bit to be set.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x224		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
9:9	RWS	0x0	outbound_poisoned_data_detect_mask:
8:8	RWS	0x0	received_msi_writes_greater_than_a_dword_data_detect_mask:
6:6	RWS	0x0	received_pcie_completion_with_ur_detect_mask:
5:5	RWS	0x0	received_pcie_completion_with_ca_detect_mask:
4:4	RWS	0x0	sent_completion_with_unsupported_request_detect_mask:

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x224		

Bit	Attr	Default	Description
3:3	RWS	0x0	sent_completion_with_completer_abort_detect_mask:
1:1	RWS	0x0	outbound_switch_fifo_data_parity_error_detect_mask:

6.2.103 xpcoredmask

XP Correctable Error Detect Mask

This register masks other correctable errors from causing the associated XPCORERRSTS status bit to be set.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x228		

Bit	Attr	Default	Description
0:0	RWS	0x0	pci_link_bandwidth_changed_detect_mask:

6.2.104 xpglberrsts

XP Global Error Status

This register captures a concise summary of the error logging in AER registers so that sideband system management software can view the errors independent of the main OS that might be controlling the AER errors.

Type: CFG	PortID: N/A	
Bus: 0	Device: 0	Function: 0
Bus: 0	Device: 2	Function: 0-3
Bus: 0	Device: 3	Function: 0-3
Offset: 0x230		

Bit	Attr	Default	Description
2:2	RW1CS	0x0	pcie_aer_correctable_error: A PCIe correctable error (ERR_COR message received from externally or through a virtual ERR_COR message generated internally) was detected anew. Note that if that error was masked in the PCIe AER, it is not reported in this field. Software clears this bit by writing a 1 and at that stage, only 'subsequent' PCIe unmasked correctable errors will set this bit.Conceptually, per the flow of PCI Express Base Spec 2.0 defined Error message control, this bit is set by the ERR_COR message that is enabled to cause a System Error notification.
1:1	RW1CS	0x0	pcie_aer_non_fatal_error: A PCIe non-fatal error (ERR_NONFATAL message received from externally or through a virtual ERR_NONFATAL message generated internally) was detected anew. Note that if that error was masked in the PCIe AER, it is not reported in this field. Software clears this bit by writing a 1 and at that stage only 'subsequent' PCIe unmasked non-fatal errors will set this bit again.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x230		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
0:0	RW1CS	0x0	pcie_aer_fatal_error: A PCIe fatal error (ERR_FATAL message received from externally or through a virtual ERR_FATAL message generated internally) was detected anew. Note that if that error was masked in the PCIe AER, it is not reported in this field. Software clears this bit by writing a 1 and at that stage, only ‘subsequent’ PCIe unmasked fatal errors will set this bit.

6.2.105 xpglberrptr

XP Global Error Pointer

Check that the perfmon registers are per “cluster”.

Type: CFG Bus: 0 Bus: 0 Bus: 0 Offset: 0x232		PortID: N/A Device: 0 Device: 2 Device: 3	Function: 0 Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
2:0	ROS_V	0x0	xp_cluster_global_first_error_pointer: This field points to which of the 3 errors indicated in the XPGLBERRSTS register happened first. This field is only valid when the corresponding status bit is set and this field is rearmed to load again when the status bit indicated to by this pointer is cleared by software from 1 to 0.Value of 0x0 corresponds to bit 0 in XPGLBERRSTS register, value of 0x1 corresponds to bit 1, and so forth.

6.2.106 pxp2cap

Secondary PCI Express Extended Capability Header.

Type: CFG Bus: 0 Bus: 0 Offset: 0x250		PortID: N/A Device: 2 Device: 3	Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x280	nxtptr: Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of capabilities.
19:16	RW_O	0x1	version: This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	RW_O	0x19	id: This field is a PCI SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h.

6.2.107 lnkcon3

Link Control 3 Register.

Type: CFG **Bus:** 0 **Bus:** 0 **Offset:** 0x254		**PortID:** N/A **Device:** 2 **Device:** 3	**Function:** 0-3 **Function:** 0-3
Bit	**Attr**	**Default**	**Description**
1:1	RW	0x0	lnkeqreqinten: Link Equalization Request Interrupt Enable. When Set, this bit enables the generation of interrupt to indicate that the Link Equalization Request bit has been set.
0:0	RW	0x0	perfeq: Performance Equalization. When this register is 1b and a 1b is written to the 'Link Retrain' register with 'Target Link Speed' set to 8GTs, the Upstream component must perform Transmitter Equalization.

6.2.108 lnerrsts

Lane Error Status Register

Type: CFG **Bus:** 0 **Bus:** 0 **Offset:** 0x258		**PortID:** N/A **Device:** 2 **Device:** 3	**Function:** 0-3 **Function:** 0-3
Bit	**Attr**	**Default**	**Description**
15:0	RW1CS	0x0	lane: A value of 1b in any bit indicates if the corresponding PCIe Express Lane detected lane based error. bit 0 Lane 0 Error Detected bit 1 Lane 1 Error Detected bit 2 Lane 2 Error Detected bit 3 Lane 3 Error Detected bit 4 Lane 4 Error Detected (not used when the link is bifurcated as x4) bit 5 Lane 5 Error Detected (not used when the link is bifurcated as x4) bit 6 Lane 6 Error Detected (not used when the link is bifurcated as x4) bit 7 Lane 7 Error Detected (not used when the link is bifurcated as x4) bit 8 Lane 8 Error Detected (not used when the link is bifurcated as x4 or x8) bit 9 Lane 9 Error Detected (not used when the link is bifurcated as x4 or x8) bit 10 Lane 10 Error Detected (not used when the link is bifurcated as x4 or x8) bit 11 Lane 11 Error Detected (not used when the link is bifurcated as x4 or x8) bit 12 Lane 12 Error Detected (not used when the link is bifurcated as x4 or x8) bit 13 Lane 13 Error Detected (not used when the link is bifurcated as x4 or x8) bit 14 Lane 14 Error Detected (not used when the link is bifurcated as x4 or x8) bit 15 Lane 15 Error Detected (not used when the link is bifurcated as x4 or x8)

6.2.109 In[0:3]eq

Lane 0 through Lane 3 Equalization Control

Type:	**CFG**	**PortID:**	**N/A**		
Bus:	**0**	**Device:**	**2**	**Function:**	**0-3**
Bus:	**0**	**Device:**	**3**	**Function:**	**0-3**
Offset:	**0x25c, 0x25e, 0x260, 0x262**				

Bit	Attr	Default	Description
14:12	RW_O	0x7	dnrxpreset: Downstream Component Receiver Preset Hint Receiver Preset Hint for Downstream Component with the following encoding. The Upstream component must pass on this value in the EQ TS2'es. 000b: -6 dB 001b: -7 dB 010b: -8 dB 011b: -9 dB 100b: -10 dB 101b: -11 dB 110b: -12 dB 111b: Reserved For a Downstream Component, this field reflects the latest Receiver Preset value requested from the Upstream Component on Lane 0. The default value is 111b.
11:8	RW_O	0x8	dntxpreset: Downstream Component Transmitter Preset Transmitter Preset for Downstream Component with the following encoding. The Upstream component must pass on this value in the EQ TS2'es. 000b: -6 dB for de-emphasis, 0 dB for preshoot 001b: -3.5 dB for de-emphasis, 0 dB for preshoot 010b: -6 dB for de-emphasis, -3.5 dB for preshoot 011b: -3.5 dB for de-emphasis, -3.5 dB for preshoot 100b: -0 dB for de-emphasis, 0 dB for preshoot 101b: -0 dB for de-emphasis, -3.5 dB for preshoot Others: reserved For a Downstream Component, this field reflects the latest Transmitter Preset requested from the Upstream Component on Lane 0. The default value is 111b.
6:4	RO	0x7	uprxpreset: Upstream Component Receiver Preset Hint Receiver Preset Hint for Upstream Component. The upstream component uses this hint for receiver equalization. The Root Ports are upstream components. The encodings are defined below. 000b: -6 dB 001b: -7 dB 010b: -8 dB 011b: -9 dB 100b: -10 dB 101b: -11 dB 110b: -12 dB 111b: reserved

Type: CFG Bus: 0 Bus: 0 Offset: 0x25c, 0x25e, 0x260, 0x262		PortID: N/A Device: 2 Device: 3	Function: 0-3 Function: 0-3
Bit	**Attr**	**Default**	**Description**
3:0	RW_O	0x8	uptxpreset: Upstream Component Transmitter Preset Transmitter Preset for an Upstream Component. The Root Ports are upstream components. The encodings are defined below. 000b: -6 dB for de-emphasis, 0 dB for preshoot 001b: -3.5 dB for de-emphasis, 0 dB for preshoot 010b: -6 dB for de-emphasis, -3.5 dB for preshoot 011b: -3.5 dB for de-emphasis, -3.5 dB for preshoot 100b: -0 dB for de-emphasis, 0 dB for preshoot 101b: -0 dB for de-emphasis, -3.5 dB for preshoot others: reserved

6.2.110 ln[4:7]eq

Lane 4 through Lane 7 Equalization Control

This register is unused when the link is configured at x4 in the bifurcation register.

Type: CFG Bus: 0 Bus: 0 Offset: 0x264, 0x266, 0x268, 0x26a		PortID: N/A Device: 2 Device: 3	Function: 0, 2 Function: 0, 2
Bit	**Attr**	**Default**	**Description**
14:12	RW_O	0x7	dnrxpreset: Downstream Component Receiver Preset Hint Receiver Preset Hint for Downstream Component with the following encoding. The Upstream component must pass on this value in the EQ TS2'es. 000b: -6 dB 001b: -7 dB 010b: -8 dB 011b: -9 dB 100b: -10 dB 101b: -11 dB 110b: -12 dB 111b: Reserved For a Downstream Component, this field reflects the latest Receiver Preset value requested from the Upstream Component on Lane 0. The default value is 111b.

Type: CFG	**PortID:** N/A		
Bus: 0	**Device:** 2	**Function:** 0, 2	
Bus: 0	**Device:** 3	**Function:** 0, 2	
Offset: 0x264, 0x266, 0x268, 0x26a			

Bit	Attr	Default	Description
11:8	RW_O	0x8	dntxpreset: Downstream Component Transmitter Preset Transmitter Preset for Downstream Component with the following encoding. The Upstream component must pass on this value in the EQ TS2'es. 000b: -6 dB for de-emphasis, 0 dB for preshoot 001b: -3.5 dB for de-emphasis, 0 dB for preshoot 010b: -6 dB for de-emphasis, -3.5 dB for preshoot 011b: -3.5 dB for de-emphasis, -3.5 dB for preshoot 100b: -0 dB for de-emphasis, 0 dB for preshoot 101b: -0 dB for de-emphasis, -3.5 dB for preshoot others: reserved For a Downstream Component, this field reflects the latest Transmitter Preset requested from the Upstream Component on Lane 0. The default value is 111b.
6:4	RO	0x7	uprxpreset: Upstream Component Receiver Preset Hint Receiver Preset Hint for Upstream Component. The upstream component uses this hint for receiver equalization. The Root Ports are upstream components. The encodings are defined below. 000b: -6 dB 001b: -7 dB 010b: -8 dB 011b: -9 dB 100b: -10 dB 101b: -11 dB 110b: -12 dB 111b: reserved
3:0	RW_O	0x8	uptxpreset: Upstream Component Transmitter Preset Transmitter Preset for an Upstream Component. The Root Ports are upstream components. The encodings are defined below. 000b: -6 dB for de-emphasis, 0 dB for preshoot 001b: -3.5 dB for de-emphasis, 0 dB for preshoot 010b: -6 dB for de-emphasis, -3.5 dB for preshoot 011b: -3.5 dB for de-emphasis, -3.5 dB for preshoot 100b: -0 dB for de-emphasis, 0 dB for preshoot 101b: -0 dB for de-emphasis, -3.5 dB for preshoot others: reserved

6.2.111 ln[8:15]eq

Lane 8 though Lane 15 Equalization Control

This register is unused when the link is configured at x4 or x8 in the bifurcation register.

Type: CFG Bus: 0 Bus: 0 Offset: 0x26c, 0x26e, 0x270, 0x272, 0x274, 0x276, 0x278, 0x27a	PortID: N/A Device: 2 Device: 3	Function: 0 Function: 0	
Bit	**Attr**	**Default**	**Description**
14:12	RW_O	0x7	dnrxpreset: Downstream Component Receiver Preset Hint Receiver Preset Hint for Downstream Component with the following encoding. The Upstream component must pass on this value in the EQ TS2'es. 000b: -6 dB 001b: -7 dB 010b: -8 dB 011b: -9 dB 100b: -10 dB 101b: -11 dB 110b: -12 dB 111b: Reserved For a Downstream Component, this field reflects the latest Receiver Preset value requested from the Upstream Component on Lane 0. The default value is 111b.
11:8	RW_O	0x8	dntxpreset: Downstream Component Transmitter Preset Transmitter Preset for Downstream Component with the following encoding. The Upstream component must pass on this value in the EQ TS2'es. 000b: -6 dB for de-emphasis, 0 dB for preshoot 001b: -3.5 dB for de-emphasis, 0 dB for preshoot 010b: -6 dB for de-emphasis, -3.5 dB for preshoot 011b: -3.5 dB for de-emphasis, -3.5 dB for preshoot 100b: -0 dB for de-emphasis, 0 dB for preshoot 101b: -0 dB for de-emphasis, -3.5 dB for preshoot others: reserved For a Downstream Component, this field reflects the latest Transmitter Preset requested from the Upstream Component on Lane 0. The default value is 111b.
6:4	RO	0x7	uprxpreset: Upstream Component Receiver Preset Hint Receiver Preset Hint for Upstream Component. The upstream component uses this hint for receiver equalization. The Root Ports are upstream components. The encodings are defined below. 000b: -6 dB 001b: -7 dB 010b: -8 dB 011b: -9 dB 100b: -10 dB 101b: -11 dB 110b: -12 dB 111b: reserved

Type: CFG	PortID: N/A	
Bus: 0	Device: 2	Function: 0
Bus: 0	Device: 3	Function: 0
Offset: 0x26c, 0x26e, 0x270, 0x272, 0x274, 0x276, 0x278, 0x27a		

Bit	Attr	Default	Description
3:0	RW_O	0x8	uptxpreset: Upstream Component Transmitter Preset Transmitter Preset for an Upstream Component. The Root Ports are upstream components. The encodings are defined below. 000b: -6 dB for de-emphasis, 0 dB for preshoot 001b: -3.5 dB for de-emphasis, 0 dB for preshoot 010b: -6 dB for de-emphasis, -3.5 dB for preshoot 011b: -3.5 dB for de-emphasis, -3.5 dB for preshoot 100b: -0 dB for de-emphasis, 0 dB for preshoot 101b: -0 dB for de-emphasis, -3.5 dB for preshoot Others: Reserved

6.3 Device 0 Function 0 Region DMIRCBAR

DMI Root Complex Registers Block (RCRB). This block is mapped into memory space, using register DMIRCBAR [Device 0:Function 0, offset 0x50].

Register Name	Offset	Size
dmivc0rcap	0x10	32
dmivc0rctl	0x14	32
dmivc0rsts	0x1a	16
dmivc1rcap	0x1c	32
dmivc1rctl	0x20	32
dmivc1rsts	0x26	16
dmivcprcap	0x28	32
dmivcprctl	0x2c	32
dmivcprsts	0x32	16
dmivcmrcap	0x34	32
dmivcmrctl	0x38	32
dmivcmrsts	0x3e	16
dmivc1cdtthrottle	0x60	32
dmivcpcdtthrottle	0x64	32
dmivcmcdtthrottle	0x68	32

6.3.1 dmivc0rcap

DMI VC0 Resource Capability

Type: MEM Bus: 0 Offset: 0x10		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RO	0x0	maxtimeslots: Max Time Slots
15:15	RO	0x0	rejsnpt: Reject Snoop Transactions 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.

6.3.2 dmivc0rctl

DMI VC0 Resource Control

Controls the resources associated with PCI Express Virtual Channel 0.

Type: MEM Bus: 0 Offset: 0x14		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RO	0x1	vc0e: Virtual Channel 0 Enable For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
26:24	RO	0x0	vc0id: Virtual Channel 0 ID Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
7:7	RO	0x0	tc7vc0m: Traffic Class 7/ Virtual Channel 0 Map Traffic Class 7 is always routed to VCm.
6:1	RW-LB	0x3f	tcvc0m: Traffic Class / Virtual Channel 0 Map Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values.For example, when bit 6 is set in this field, TC6 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0:0	RO	0x1	tc0vc0m: Traffic Class 0 / Virtual Channel 0 Map Traffic Class 0 is always routed to VC0.

6.3.3 dmivc0rsts

DMI VC0 Resource Status.

Reports the Virtual Channel specific status.

Type: MEM Bus: 0 Offset: 0x1a	PortID: 8'h7e Device: 0	Function: 0	
Bit	**Attr**	**Default**	**Description**
1:1	RO-V	0x1	vc0np: Virtual Channel 0 Negotiation Pending 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.

6.3.4 dmivc1rcap

DMI VC1 Resource Capability

Type: MEM Bus: 0 Offset: 0x1c	PortID: 8'h7e Device: 0	Function: 0	
Bit	**Attr**	**Default**	**Description**
15:15	RO	0x1	rejsnpt: Reject Snoop Transactions 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.

6.3.5 dmivc1rctl

DMI VC1 Resource Control

Controls the resources associated with PCI Express Virtual Channel 1.

Type: MEM Bus: 0 Offset: 0x20		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW-LB	0x0	vc1e: Virtual Channel 1 Enable 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
26:24	RW-LB	0x1	vc1id: Virtual Channel 1 ID Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
7:7	RO	0x0	tc7vc1m: Traffic Class 7/ Virtual Channel 1 Map Traffic Class 7 is always routed to VCm.
6:1	RW-LB	0x0	tcvc1m: Traffic Class / Virtual Channel 1 Map Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values.For example, when bit 6 is set in this field, TC6 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0:0	RO	0x0	tc0vc1m: Traffic Class 0 / Virtual Channel 0 Map Traffic Class 0 is always routed to VC0.

6.3.6 dmivc1rsts

DMI VC1 Resource Status

Reports the Virtual Channel specific status.

Type: MEM Bus: 0 Offset: 0x26			PortID: 8'h7e Device: 0 Function: 0
Bit	**Attr**	**Default**	**Description**
1:1	RO-V	0x1	vc1np: Virtual Channel 1 Negotiation Pending 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.

6.3.7 dmivcprcap

DMI VCP Resource Capability

Type: MEM Bus: 0 Offset: 0x1a			PortID: 8'h7e Device: 0 Function: 0
Bit	**Attr**	**Default**	**Description**
15:15	RO	0x0	rejsnpt: Reject Snoop Transactions 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.

6.3.8 dmivcprctl

DMI VCP Resource Control

Controls the resources associated with the DMI Private Channel (VCp).

Type: MEM Bus: 0 Offset: 0x1a		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW-LB	0x0	vcpe: Virtual Channel Private Enable 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
26:24	RW-LB	0x2	vcpid: Virtual Channel Private ID Assigns a VC ID to the VC resource. This field can not be modified when the VC is already enabled. No private VCs are precluded by hardware and private VC handling is implemented the same way as non-private VC handling.
7:7	RO	0x0	tc7vcpm: Traffic Class 7/ Virtual Channel 0 Map Traffic Class 7 is always routed to VCm.
6:1	RW-LB	0x0	tcvcpm: Traffic Class / Virtual Channel private Map Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values.For example, when bit 6 is set in this field, TC6 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0:0	RO	0x0	tc0vcpm: Traffic Class 0 / Virtual Channel Private Map Traffic Class 0 is always routed to VC0.

6.3.9 dmivcprsts

DMI VCP Resource Status

Reports the Virtual Channel specific status.

Type: MEM Bus: 0 Offset: 0x32		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
1:1	RO-V	0x1	vcpnp: Virtual Channel Private Negotiation Pending 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.

6.3.10 dmivcmrcap

DMI VCM Resource Capability

Type: MEM Bus: 0 Offset: 0x34		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
15:15	RO	0x1	rejsnpt: Reject Snoop Transactions 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.

6.3.11 dmivcmrctl

DMI VCM Resource Control

Controls the resources associated with PCI Express Virtual Channel 0.

Type: MEM	PortID: 8'h7e	
Bus: 0	Device: 0	Function: 0
Offset: 0x38		

Bit	Attr	Default	Description
31:31	RW-LB	0x0	vcme: Virtual Channel M Enable 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
26:24	RW-LB	0x0	vcmid: VCm ID
7:7	RO	0x1	tc7vcpm: Traffic Class 7/ Virtual Channel 0 Map Traffic Class 7 is always routed to VCm.
6:1	RO	0x0	tcvcmm: Traffic Class / Virtual Channel M Map No other traffic class is mapped to VCM
0:0	RO	0x0	tc0vcmm: Traffic Class 0 Virtual Channel Map

6.3.12 dmivimrsts

DMI VCM Resource Status

Reports the Virtual Channel specific status.

Type: MEM Bus: 0 Offset: 0x3e		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
1:1	RO-V	1b	vcmnp: Virtual Channel M Negotiation Pending 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.

6.3.13 dmivc1cdtthrottle

DMI VC1 Credit Throttle

Type: MEM Bus: 0 Offset: 0x60		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:24	RWS	0x0	prd: Posted Request Data VC1 Credit Withhold Number of VC1 Posted Data credits to withhold from being reported or used.
21:16	RWS	0x0	prh: Posted Request Header VC1 Credit Withhold Number of VC1 Posted Request credits to withhold from being reported or used.
15:8	RWS	0x0	nprd: Non-Posted Request Data VC1 Credit Withhold Number of VC1 Non-Posted Data credits to withhold from being reported or used.
5:0	RWS	0x0	nprh: Non-Posted Request Header VC1 Credit Withhold Number of VC1 Non-Posted Request credits to withhold from being reported or used.

6.3.14 dmivcpcdtthrottle

DMI VCp Credit Throttle

Type: MEM Bus: 0 Offset: 0x64		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:24	RWS	0x0	prd: Posted Request Data VCp Credit Withhold Number of VCp Posted Data credits to withhold from being reported or used.
21:16	RWS	0x0	prh: Posted Request Header VCp Credit Withhold Number of VCp Posted Request credits to withhold from being reported or used.
15:8	RWS	0x0	nprd: Non-Posted Request Data VCp Credit Withhold Number of VCp Non-Posted Data credits to withhold from being reported or used.
5:0	RWS	0x0	nprh: Non-Posted Request Header VCp Credit Withhold Number of VCp Non-Posted Request credits to withhold from being reported or used.

6.3.15 dmivcmcdtthrottle

DMI VCm Credit Throttle

Type: MEM Bus: 0 Offset: 0x68		PortID: 8'h7e Device: 0	Function: 0
Bit	**Attr**	**Default**	**Description**
31:24	RWS	0x0	prd: Posted Request Data VCm Credit Withhold Number of VCm Posted Data credits to withhold from being reported or used.
21:16	RWS	0x0	prh: Posted Request Header VCm Credit Withhold Number of VCm Posted Request credits to withhold from being reported or used.
15:8	RWS	0x0	nprd: Non-Posted Request Data VCm Credit Withhold Number of VCm Non-Posted Data credits to withhold from being reported or used.
5:0	RWS	0x0	nprh: Non-Posted Request Header VCm Credit Withhold Number of VCm Non-Posted Request credits to withhold from being reported or used.

6.4 Device 4 Function 0-7

Intel® QuickData Technology DMA Registers.

Register Name	Offset	Size	Function
vid	0x0	16	0-7
did	0x2	16	0-7
pcicmd	0x4	16	0-7
pcists	0x6	16	0-7
rid	0x8	8	0-7
ccr	0x9	24	0-7
clsr	0xc	8	0-7
hdr	0xe	8	0-7
cb_bar	0x10	64	0-7
svid	0x2c	16	0-7
sdid	0x2e	16	0-7
capptr	0x34	8	0-7
intl	0x3c	8	0-7
intpin	0x3d	8	0-7
devcfg	0x60	16	0
msixcapid	0x80	8	0-7
msixnxtptr	0x81	8	0-7
msixmsgctl	0x82	16	0-7
tableoff_bir	0x84	32	0-7
pbaoff_bir	0x88	32	0-7
capid	0x90	8	0-7
nextptr	0x91	8	0-7
expcap	0x92	16	0-7
devcap	0x94	32	0-7
devcon	0x98	16	0-7
devsts	0x9a	16	0-7
devcap2	0xb4	32	0-7
devcon2	0xb8	16	0-7
pmcap	0xe0	32	0-7
pmcsr	0xe4	32	0-7
dmauncerrsts	0x148	32	0
dmauncerrmsk	0x14c	32	0
dmauncerrsev	0x150	32	0
dmauncerrptr	0x154	8	0
dmaglberrptr	0x160	8	0
chanerr_int	0x180	32	0-7
chanerrmsk_int	0x184	32	0-7
chanerrsev_int	0x188	32	0-7
chanerrptr	0x18c	8	0-7

6.4.1 vid

Type: CFG Bus: 0 Offset: 0x0		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x8086	vendor_identification_number: The value is assigned by PCI-SIG to Intel.

6.4.2 did

Type: CFG Bus: 0 Offset: 0x2		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x2f20 (Function 0) 0x2f21 (Function 1) 0x2f22 (Function 2) 0x2f23 (Function 3) 0x2f24 (Function 4) 0x2f25 (Function 5) 0x2f26 (Function 6) 0x2f27 (Function 7)	device_identification_number: Device ID values vary from function to function.

6.4.3 pcicmd

Type: CFG Bus: 0 Offset: 0x4		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
10:10	RW	0x0	intx_interrupt_disable:
9:9	RO	0x0	fast_back_to_back_enable: Not applicable to PCI Express and is hardwired to 0
8:8	RO	0x0	serre:
7:7	RO	0x0	idsel_stepping_wait_cycle_control: Not applicable to internal devices. Hardwired to 0.
6:6	RO	0x0	perre:
5:5	RO	0x0	vga_palette_snoop_enable: Not applicable to internal devices. Hardwired to 0.
4:4	RO	0x0	mwie:
3:3	RO	0x0	sce:
2:2	RW	0x0	bme:
1:1	RW	0x0	mse:
0:0	RO	0x0	iose:

6.4.4 pcists

Type: CFG Bus: 0 Offset: 0x6		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:15	RW1C	0x0	dpe:
14:14	RO	0x0	sse:
13:13	RO	0x0	rma:
12:12	RO	0x0	rta:
11:11	RW1C	0x0	sta:
10:9	RO	0x0	devsel_timing: Not applicable to PCI Express. Hardwired to 0.
8:8	RW1C	0x0	mdpe:
7:7	RO	0x0	fast_back_to_back: Not applicable to PCI Express. Hardwired to 0.
5:5	RO	0x0	pci66mhz_capable: Not applicable to PCI Express. Hardwired to 0.
4:4	RO	0x1	capabilities_list: This bit indicates the presence of a capabilities list structure
3:3	RO_V	0x0	intxsts:

6.4.5 rid

Type: CFG Bus: 0 Offset: 0x8		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register in any Intel® Xeon® Processor E7 v4 product family function.

6.4.6 ccr

Type: CFG Bus: 0 Offset: 0x9		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
23:16	RO_V	0x8	base_class: Generic Device
15:8	RO_V	0x80	sub_class: Generic Device
7:0	RO_V	0x0	register_level_programming_interface: Set to 00h for all non-APIC devices.

6.4.7 clsr

Type: CFG Bus: 0 Offset: 0xc		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	cacheline_size: This register is set as RW for compatibility reasons only. Cacheline size is always 64B.

6.4.8 hdr

Type: CFG Bus: 0 Offset: 0xe		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:7	RO	0x1	multi_function_device: This bit defaults to 1b since all these devices are multi-function
6:0	RO	0x0	configuration_layout: This field identifies the format of the configuration header layout. It is Type 0 for all these devices. The default is 00h, indicating a 'endpoint device'.

6.4.9 cb_bar

Intel QuickData Technology Base Address Register.

Type: CFG Bus: 0 Offset: 0x10		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
63:14	RW	0x0	bar: This marks the 16 KB aligned 64-bit base address for memory-mapped registers of Intel QuickData Technology-DMA. The BAR register in the 8 functions will be referenced with a logical name of CB_BAR[0:7].
3:3	RO	0x0	prefetchable: The DMA registers are not prefetchable.
2:1	RO	0x2	type: The DMA registers is 64-bit address space and can be placed anywhere within the addressable region of the system.
0:0	RO	0x0	memory_space: This Base Address Register indicates memory space.

6.4.10 svid

Type: CFG Bus: 0 Offset: 0x2c		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x8086	vendor_identification_number:

6.4.11 sdid

Type: CFG Bus: 0 Offset: 0x2e		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x0	subsystem_identification_number:

6.4.12 capptr

Type: CFG Bus: 0 Offset: 0x34		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x80	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.

6.4.13 intl

Type: CFG Bus: 0 Offset: 0x3c		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	interrupt_line: NA for these devices

6.4.14 intpin

Type: CFG Bus: 0 Offset: 0x3d	PortID: N/A Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
7:0	RW_O	0x1 (Function 0) 0x2 (Function 1) 0x3 (Function 2) 0x4 (Function 3) 0x1 (Function 4) 0x2 (Function 5) 0x3 (Function 6) 0x4 (Function 7)	cb_intpin0: (Function 0) cb_intpin1: (Function 1) cb_intpin2: (Function 2) cb_intpin3: (Function 3) cb_intpin4: (Function 4) cb_intpin5: (Function 5) cb_intpin6: (Function 6) cb_intpin7: (Function 7)

6.4.15 devcfg

This DEVCFG is for Function 0 only

Type: CFG Bus: 0 Offset: 0x60	PortID: N/A Device: 4	Function: 0	
Bit	**Attr**	**Default**	**Description**
11:11	RW_O	0x0	f1extop_diden: When set, this bit switches in the Function 1 Device ID that are typically used in storage applications. When clear, the function 1 DID remains at the default value associated with applications (for example, networking). This bit should be written by BIOS prior to enumeration.
10:10	RW_O	0x0	f0extop_diden: When set, this bit switches in the Function 0 Device ID that are typically used in storage applications. When clear, the function 0 DID remains at the default value associated with applications (e.g.,networking). This bit should be written by BIOS prior to enumeration.
9:9	RWS	0x0	enable_no_snoop: This bit is akin to the NoSnoop enable bit in the PCI Express capability register, only that this bit is controlled by bios rather than OS. When set, the no snoop optimization is enabled (provided the equivalent bit in the PCI Express DEVCON register is set) on behalf of Intel QuickData Technology DMA otherwise it is not. Notes: Due to severe performance degradation, it is not recommended that this bit be set except in debug mode.

6.4.16 msixcapid

MSI-X Capability ID.

Type: CFG Bus: 0 Offset: 0x80	PortID: N/A Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x11	cb_msixcapid: Assigned by PCI-SIG for MSI-X (Intel QuickData Technology DMA)

6.4.17 msixnxtptr

MSI-X Next Pointer.

Type: CFG Bus: 0 Offset: 0x81	PortID: N/A Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x90	cb_msixnxtptr: This field is set to 90h for the next capability list (PCI Express capability structure) in the chain.

6.4.18 msixmsgctl

MSI-X Message Control.

Type: CFG Bus: 0 Offset: 0x82	PortID: N/A Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:15	RW	0x0	msi_x_enable: Software uses this bit to select between MSI-X or INTx method for signaling interrupts from the DMA 0: INTx method is chosen for DMA interrupts 1: MSI-X method is chosen for DMA interrupts
14:14	RW	0x0	function_mask: If 1, the 1 vector associated with the dma is masked, regardless of the per-vector mask bit state. If 0, the vector's mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X function mask bit has no effect on the state of the per-vector Mask bit.
10:0	RO	0x0	table_size: Indicates the MSI-X table size which for IIO is 1, encoded as a value of 0h.

6.4.19 tableoff_bir

MSI-X Table Offset and BAR Indicator.

Type: CFG Bus: 0 Offset: 0x84	PortID: N/A Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:3	RO	0x400	table_offset: MSI-X Table Structure is at offset 8K from the Intel QuickData Technology BAR address. See “MSI-X Lower Address Registers (MSGADDR)” for the start of details relating to MSI-X registers.
2:0	RO	0x0	table_bir: Intel QuickData Technology DMA BAR is at offset 10h in the DMA config space and hence this register is 0.

6.4.20 pbaoff_bir

Type: CFG Bus: 0 Offset: 0x88			PortID: N/A Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:3	RO	0x600	table_offset: MSI-X PBA Structure is at offset 12K from the Intel QuickData Technology BAR address.
2:0	RO	0x0	table_bir: Intel QuickData Technology DMA BAR is at offset 10h in the DMA config space and hence this register is 0.

6.4.21 capid

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 3.0 configuration space

Type: CFG Bus: 0 Offset: 0x90			PortID: N/A Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x10	capability_id: Provides the PCI Express capability ID assigned by PCI-SIG.

6.4.22 nextptr

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 3.0 configuration space

Type: CFG Bus: 0 Offset: 0x91			PortID: N/A Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO	0xe0	next_ptr: This field is set to the PCI Power Management capability.

6.4.23 expcap

The PCI Express Capabilities register identifies the PCI Express device type and associated capabilities

Type: CFG Bus: 0 Offset: 0x92			PortID: N/A Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
13:9	RO	0x0	interrupt_message_number: N/A

Type: CFG Bus: 0 Offset: 0x92		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
8:8	RO	0x0	slot_implemented: N/A
7:4	RO	0x9	device_port_type: This field identifies the type of device. It is set to for the DMA to indicate root complex integrated endpoint device.
3:0	RO	0x2	capability_version: This field identifies the version of the PCI Express capability structure. Set to 2h for PCI Express and DMA devices for compliance with the extended base registers.

6.4.24 devcap

The PCI Express Device Capabilities register identifies device specific information for the device.

Type: CFG Bus: 0 Offset: 0x94		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
28:28	RWS_O	0x0	flr_supported:
27:26	RO	0x0	captured_slot_power_limit_scale: Does not apply to Intel QuickData Technology DMA
25:18	RO	0x0	captured_slot_power_limit_value: Does not apply to Intel QuickData Technology DMA
15:15	RO	0x1	role_based_error_reporting: IIO is 1.1 compliant and so supports this feature
14:14	RO	0x0	power_indicator_present_on_device: Does not apply to Intel QuickData Technology DMA
13:13	RO	0x0	attention_indicator_present: Does not apply to Intel QuickData Technology DMA
12:12	RO	0x0	attention_button_present: Does not apply to Intel QuickData Technology DMA
11:9	RO	0x0	endpoint_l1_acceptable_latency: N/A
8:6	RO	0x0	endpoint_l0s_acceptable_latency: N/A
5:5	RO	0x0	extended_tag_field_supported:
4:3	RO	0x0	phantom_functions_supported: Intel QuickData Technology DMA does not support phantom functions.
2:0	RO	0x0	max_payload_size: Intel QuickData Technology DMA supports max 128B on writes to PCI Express

6.4.25 devcon

The PCI Express Device Control register controls PCI Express specific capabilities parameters associated with the device.

Type: CFG	PortID: N/A		
Bus: 0	Device: 4	Function: 0-7	
Offset: 0x98			

Bit	Attr	Default	Description
15:15	RW	0x0	initiate_flr: Intel QuickData Technology DMA does a reset of that function only per the FLR ECN. This bit always returns 0 when read and a write of 0 has no impact
14:12	RO	0x0	max_read_request_size: N/A to Intel QuickData Technology DMA since it does not issue tx on PCIe
11:11	RW	0x1	enable_no_snoop: For Intel QuickData Technology DMA, when this bit is clear, all DMA transactions must be snooped. When set, DMA transactions to main memory can utilize No Snoop optimization under the guidance of the device driver.
10:10	RO	0x0	auxiliary_power_management_enable: Not applicable to Intel QuickData Technology DMA
9:9	RO	0x0	phantom_functions_enable: Not applicable to Intel QuickData Technology DMA since it never uses phantom functions as a requester.
8:8	RO	0x0	extended_tag_field_enable:
7:5	RO	0x0	max_payload_size: N/A for Intel QuickData Technology DMA
4:4	RW	0x0	enable_relaxed_ordering: For most parts, writes from Intel QuickData Technology DMA are relaxed ordered, except for DMA completion writes. But the fact that Intel QuickData Technology DMA writes are relaxed ordered is not very useful except when the writes are also non-snooped. If the writes are snooped, relaxed ordering does not provide any particular advantage based on IIO uArch. But when writes are non-snooped, relaxed ordering is required to get good BW and this bit is expected to be set. If this bit is clear, NS writes will get terrible performance.
3:3	RO	0x0	unsupported_request_reporting_enable: N/A for Intel QuickData Technology DMA
2:2	RO	0x0	fatal_error_reporting_enable: N/A for Intel QuickData Technology DMA
1:1	RO	0x0	non_fatal_error_reporting_enable: N/A for Intel QuickData Technology DMA
0:0	RO	0x0	correctable_error_reporting_enable: N/A for Intel QuickData Technology DMA

6.4.26 devsts

The PCI Express Device Status register provides information about PCI Express device specific parameters associated with the device

Type: CFG Bus: 0 Offset: 0x9a		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
5:5	RO	0x0	transactions_pending: 1: indicates that the Intel QuickData Technology DMA device has outstanding Non-Posted Request which it has issued either towards main memory, which have not been completed. 0: Intel QuickData Technology DMA reports this bit cleared only when all Completions for any outstanding Non-Posted Requests it owns have been received.
4:4	RO	0x0	aux_power_detected: Does not apply to IIO
3:3	RO	0x0	unsupported_request_detected: N/A for Intel QuickData Technology DMA
2:2	RO	0x0	fatal_error_detected: N/A for Intel QuickData Technology DMA
1:1	RO	0x0	non_fatal_error_detected: N/A for Intel QuickData Technology DMA
0:0	RO	0x0	correctable_error_detected: N/A for Intel QuickData Technology DMA

6.4.27 devcap2

Type: CFG Bus: 0 Offset: 0xb4		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:4	RO	0x1	completion_timeout_disable_supported:
3:0	RO	0x0	completion_timeout_values_supported: Not Supported

6.4.28 devcon2

Type: CFG Bus: 0 Offset: 0xb8		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:4	RW	0x0	completion_timeout_disable:
3:0	RO	0x0	completion_timeout_value:

6.4.29 pmcap

Power Management Capability.

The Power Management Capabilities Register defines the capability ID, next pointer and other power management related support. The following Power Management registers / capabilities are added for software compliance.

Type: CFG Bus: 0 Offset: 0xe0		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
26:26	RO	0x0	d2_support: Does not support power management state D2.
25:25	RO	0x0	d1_support: Does not support power management state D1.
24:22	RO	0x0	aux_current:
21:21	RO	0x0	device_specific_initialization:
19:19	RO	0x0	pme_clock: This field is hardwired to 0h as it does not apply to PCI Express.
18:16	RWS_O	0x3	version: This field is set to 3h (Power Management 1.2 compliant) as version number. Bit is RW-O to make the version 2h incase legacy OS'es have any issues.
15:8	RO	0x0	next_capability_pointer: This is the last capability in the chain and hence set to 0.
7:0	RO	0x1	capability_id: Provides the Power Management capability ID assigned by PCI-SIG.

6.4.30 pmcsr

Power Management Control and Status.

This register provides status and control information for Power Management events in the PCI Express port of the IIO.

Type: CFG Bus: 0 Offset: 0xe4		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:24	RO	0x0	data: N/A
23:23	RO	0x0	bus_power_clock_control_enable: N/A
22:22	RO	0x0	b2_b3_support: N/A
15:15	RO	0x0	pme_status: N/A
14:13	RO	0x0	data_scale: N/A
12:9	RO	0x0	data_select: N/A

Type: CFG Bus: 0 Offset: 0xe4		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
8:8	RO	0x0	pme_enable: N/A
3:3	RO	0x1	no_soft_reset: Indicates does not reset its registers when transitioning from D3hot to D0.
1:0	RW_V	0x0	power_state: This 2-bit field is used to determine the current power state of the function and to set a new power state as well. 00: D0 01: D1 (not supported by IOAPIC) 10: D2 (not supported by IOAPIC) 11: D3_hot If Software tries to write 01 or 10 to this field, the power state does not change from the existing power state which is either (D0 or D3_hot) and nor do these bits[1:0] change value. When in D3_hot state, IOxAPIC will a) respond to only Type 0 configuration transactions targeted at the device's configuration space, when in D3_hot state c) will not respond to memory i.e. D3hot state is equivalent to MSE , accesses to MBAR region note: ABAR region access still go through in D3_hot state, if it enabled d) will not generate any MSI writes

6.4.31 dmauncerrsts

DMA Cluster Uncorrectable Error Status.

Type: CFG Bus: 0 Offset: 0x148		PortID: N/A Device: 4	Function: 0
Bit	**Attr**	**Default**	**Description**
12:12	RW1CS	0x0	syndrome: Multiple errors
10:10	RW1CS	0x0	read_address_decode_error_status:
7:7	RW1CS	0x0	rd_cmpl_header_error_status:
3:3	RW1CS	0x0	dma_internal_hw_parity_error_status:
2:2	RW1CS	0x0	received_poisoned_data_from_dp_status:

6.4.32 dmauncerrmsk

DMA Cluster Uncorrectable Error Mask.

Type: CFG Bus: 0 Offset: 0x14c	PortID: N/A Device: 4	Function: 0	
Bit	**Attr**	**Default**	**Description**
12:12	RWS	0x0	syndrome: Multiple errors
10:10	RWS	0x0	read_address_decode_error_mask:
7:7	RWS	0x0	rd_cmpl_header_error_mask:
4:4	RWS	0x0	cfg_reg_parity_error_mask:
3:3	RWS	0x0	dma_internal_hw_parity_error_mask:
2:2	RWS	0x0	received_poisoned_data_from_dp_mask:

6.4.33 dmauncerrsev

DMA Cluster Uncorrectable Error Severity.

This register controls severity of uncorrectable DMA unit errors between fatal and non-fatal.

Type: CFG Bus: 0 Offset: 0x150	PortID: N/A Device: 4	Function: 0	
Bit	**Attr**	**Default**	**Description**
12:12	RWS	0x0	syndrome: Multiple errors
10:10	RWS	0x0	read_address_decode_error_severity:
7:7	RWS	0x1	rd_cmpl_header_error_severity:
4:4	RWS	0x1	cfg_reg_parity_error_severity:
3:3	RWS	0x1	dma_internal_hw_parity_error_severity:
2:2	RWS	0x0	received_poisoned_data_from_dp_severity:

6.4.34 dmauncerrptr

DMA Cluster Uncorrectable Error Pointer..

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0
Offset: 0x154		

Bit	Attr	Default	Description
4:0	ROS_V	0x0	uncerrptr: Points to the first unmasked uncorrectable error logged in the DMAUNCERRSTS register. This field is only valid when the corresponding error is unmasked and the status bit is set and this register is rearmed to load again once the error pointed by this field in the uncorrectable error status register is cleared.Value of 0x0 corresponds to bit 0 in DMAUNCERRSTS register, value of 0x1 corresponds to bit 1 etc.

6.4.35 dmaglberrptr

DMA Cluster Global Error Pointer.

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0
Offset: 0x160		

Bit	Attr	Default	Description
3:0	ROS_V	0x0	global_error_pointer: Points to one of 8 possible sources of uncorrectable errors – DMA channels 0-7. The DMA channel errors are logged in CHANERRx_INT registers. This register is only valid when the register group pointed to by this register has at least one unmasked error status bit set and this register is rearmed to load again once all the unmasked uncorrectable errors in the source pointed to by this field are cleared. Value of 0x0 corresponds to channel#0, value of 0x1 corresponds to channel#1, and value of 0x7 corresponds to channel#7

6.4.36 chanerr_int

Internal DMA Channel Error Status Registers.

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x180		

Bit	Attr	Default	Description
18:18	RW1CS (Function 0-1) RO (Function 2-7)	0x0	desccnterr: (Function 0-1) The hardware sets this bit when it encounters a base descriptor that requires an extended descriptor (such as an XOR with 8 sources), but DMACount indicates that the Base descriptor is the last descriptor that can be processed. Reserved. (Function 2-7)
17:17	RW1CS (Function 0-1) RO (Function 2-7)	0x0	xorqerr: The hardware sets this bit when the Q validation part of the XOR with Galois Field Multiply Validate operation fails. Reserved. (Function 2-7)
16:16	RW1CS	0x0	crc_xorp_err: The hardware sets this bit when a CRC Test operation or XOR Validity operation fails or when the P validation part of the XOR with Galois Field Multiply Validate operation fails.

Type: CFG Bus: 0 Offset: 0x180		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:15	RO	0x0	unaffil_err: Unaffiliated Error. IIO never sets this bit
14:14	RO	0x0	unused:
13:13	RW1CS	0x0	int_cfg_err: Interrupt Configuration Error. The DMA channel sets this bit indicating that the interrupt registers were not configured properly when the DMA channel attempted to generate an interrupt e.g. interrupt address is not 0xFEE.
12:12	RW1CS	0x0	cmp_addr_err: Completion Address Error. The DMA channel sets this bit indicating that the completion address register was configured to an illegal address or has not been configured.
11:11	RW1CS	0x0	desc_len_err: Descriptor Length Error. The DMA channel sets this bit indicating that the current transfer has an illegal length field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
10:10	RW1CS	0x0	desc_ctrl_err: Descriptor Control Error. The DMA channel sets this bit indicating that the current transfer has an illegal control field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
9:9	RW1CS	0x0	wr_data_err: Write Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while writing the destination data. This error could be because of an internal ram error in the write queue that stores the write data before being written to main memory. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
8:8	RW1CS	0x0	rd_data_err: Read Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while accessing the source data. This error could be a read data that is received poisoned. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
7:7	RW1CS	0x0	dma_data_parerr: DMA Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered an uncorrectable ECC/parity error reported by the DMA engine.
6:6	RW1CS	0x0	cdata_parerr: Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered a parity error. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
5:5	RW1CS	0x0	chancmd_err: CHANCMD Error. The DMA channel sets this bit indicating that a write to the CHANCMD register contained an invalid value (e.g. more than one command bit set).
4:4	RW1CS	0x0	chn_addr_valerr: Chain Address Value Error. The DMA channel sets this bit indicating that the CHAINADDR register has an illegal address including an alignment error (not on a 64-byte boundary).

Type: CFG Bus: 0 Offset: 0x180		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
3:3	RW1CS	0x0	descriptor_error: The DMA channel sets this bit indicating that the current transfer has encountered an error (not otherwise covered under other error bits) when reading or executing a DMA descriptor. When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
2:2	RW1CS	0x0	nxt_desc_addr_err: Next Descriptor Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal next descriptor address including an alignment error (not on a 64-byte boundary). When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
1:1	RW1CS	0x0	dma_xfrer_daddr_err: DMA Transfer Destination Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal destination address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.
0:0	RW1CS	0x0	dma_trans_saddr_err: DMA Transfer Source Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal source address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.

6.4.37 chanerrmsk_int

Internal DMA Channel Error Mask Registers.

Type: CFG Bus: 0 Offset: 0x184		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RWS (Function 0-1) RO (Function 2-7)	0x0	mask18: This register is a bit for bit mask for the CHANERR_INT register 0: enable 1: disable
17:17	RWS (Function 0-1) RO (Function 2-7)	0x0	mask17: This register is a bit for bit mask for the CHANERR_INT register 0: enable 1: disable
16:16	RWS	0x0	mask16: This register is a bit for bit mask for the CHANERR_INT register 0: enable 1: disable
15:15	RO	0x0	chanerrintmskro:
13:0	RWS	0x0	mask13_0: This register is a bit for bit mask for the CHANERR_INT register 0: enable 1: disable

6.4.38 chanerrsev_int

Internal DMA Channel Error Severity Registers.

Type: CFG Bus: 0 Offset: 0x188	PortID: N/A Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RWS (Function 0-1) RO (Function 2-7)	0x0	severity18: (Function 0-1) 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic. Reserved. (Function 2-7)
17:17	RWS (Function 0-1) RO (Function 2-7)	0x0	severity17: (Function 0-1) 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic. Reserved. (Function 2-7)
16:16	RWS	0x0	severity16: 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic.
15:14	RO	0x0	chanerrsevro1_0:
13:0	RWS	0x0	severity13_0: 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic.

6.4.39 chanerrptr

DMA Channel Error Pointer.

Type: CFG Bus: 0 Offset: 0x18c	PortID: N/A Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:0	ROS_V	0x0	dma_chan_err_pointer: Points to the first uncorrectable, unmasked error logged in the CHANERR_INT register. This register is only valid when the corresponding error is unmasked and its status bit is set and this register is rearmed to load again once the error pointed to by this register, in the CHANERR_INT status register, is cleared.

6.5 Device 4 Function 0 - 7 MMIO Region Intel QuickData Technology BARs

Intel QuickData Technology MMIO Register used to control the DMA functionality. The Intel QuickData Technology BAR register points to the based address to these registers.

All of these registers are accessible from only the processor. The IIO supports accessing the Intel® QuickData Technology device memory-mapped registers via QWORD reads and writes. The offsets indicated in the following table are from the Intel® QuickData Technology BAR value.

Register Name	Offset	Size
chancnt	0x0	8
xfercap	0x1	8
genctrl	0x2	8
intrctrl	0x3	8
attnstatus	0x4	32
cbver	0x8	8
intrdelay	0xc	16
cs_status	0xe	16
dmacapability	0x10	32
dcaoffset	0x14	16
cbprio	0x40	8
chanctrl	0x80	16
dma_comp	0x82	16
chancmd	0x84	8
dmacount	0x86	16
chansts_0	0x88	32
chansts_1	0x8c	32
chainaddr_0	0x90	32
chainaddr_1	0x94	32
chancmp_0	0x98	32
chancmp_1	0x9c	32
chanerr	0xa8	32
chanerrmsk	0xac	32
dcactrl	0xb0	32
dca_ver	0x100	8
dca_reqid_offset	0x102	16
csi_capability	0x108	16
pcie_capability	0x10a	16
csi_cap_enable	0x10c	16
pcie_cap_enable	0x10e	16
apicid_tag_map	0x110	64
dca_reqid0	0x180	32
dca_reqid1	0x184	32
msgaddr	0x2000	32

Register Name	Offset	Size
msgupaddr	0x2004	32
msgdata	0x2008	32
vecctrl	0x200c	32
pendingbits	0x3000	32

6.5.1 chancnt

Channel Count.

The Channel Count register specifies the number of channels that are implemented.

Type: MEM Bus: 0 Offset: 0x0		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:0	RO	0x1	num_chan: Number of channels. Specifies the number of DMA channels. The IIO supports 1 DMA Channel per function so this register will always read 1.

6.5.2 xfercap

Transfer Capacity.

The Transfer Capacity specifies the minimum of the maximum DMA transfer size supported on all channels.

Type: MEM Bus: 0 Offset: 0x1		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:0	RO	0x14	trans_size: Transfer size. This field specifies the number of bytes that may be specified in a DMA descriptor's Transfer Size field. This defines the maximum transfer size supported by IIO as a power of 2. CPU will support 1M max.

6.5.3 genctrl

DMA General Control.

The DMA Control register provides for general control operations.

Type: MEM Bus: 0 Offset: 0x2		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x0	dbgen: Debug Enable

6.5.4 intrctrl

The Interrupt Control register provides for control of DMA interrupts.

Type: MEM Bus: 0 Offset: 0x3		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
3:3	RW	0x0	msix_vecctrl: Intel QuickData Technology DMA ignores this bit
2:2	RO	0x0	intp: Interrupt. This bit is set whenever the channel status bit in the Attention Status register is set and the Master Interrupt Enable bit is set. That is, it is the logical AND of Interrupt Status and Master Interrupt Enable bits of this register. This bit represents the legacy interrupt drive signal (when in legacy interrupt mode). In MSI-X mode, this bit is not used by software and is a don't care.
1:1	RO	0x0	intp_sts: Interrupt Status. This bit is set whenever the bit in the Attention Status register is set. This bit is not used by software in MSI-X mode and is a don't care.
0:0	RW	0x0	mstr_intp_en: Master Interrupt Enable. Setting this bit enables the generation of an interrupt in legacy interrupt mode. This bit is automatically reset each time this register is read. When this bit is clear ed, the IIO will not generate a legacy interrupt under otherwise valid conditions. This bit is not used when DMA is in MSI-X mode.

6.5.5 attnstatus

Attention Status.

Type: MEM Bus: 0 Offset: 0x4		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RO_V	0x0	chanattn: Channel Attention. Represents the interrupt status of the channel. This bit clears when read. Writes have no impact on this bit.

6.5.6 cbver

The Intel® QuickData Technology version register field indicates the version of the Intel QuickData Technology specification that the IIO implements. The most significant 4-bits (range 7:4) are the major version number and the least significant 4-bits (range 3:0) are the minor version number. The IIO implementation for this Intel QuickData Technology version is 3.2 encoded as 0b0011 0010.

Type: MEM Bus: 0 Offset: 0x8	PortID: 8'h7e Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:4	RO	0x3	mjrver: Major Version. Specifies Major version of the Intel QuickData Technology implementation. Current value is 2h
3:0	RO	0x2	mnrver: Minor Version. Specifies Minor version of the Intel QuickData Technology implementation. Current value is 0h

6.5.7 intrdelay

Interrupt Delay.

Type: MEM Bus: 0 Offset: 0xc	PortID: 8'h7e Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:15	RO	0x1	interrupt_coalescing_supported: The IIO does support interrupt coalescing by delaying interrupt generation.
13:0	RW	0x0	interrupt_delay_time: Specifies the number of microseconds that the IIO delays generation of an interrupt (legacy or MSI or MSI-X) from the time that interrupts are enabled (That is, Master Interrupt Enable bit in the CSIPINTRCTRL register is set or, for MSI-X when Vector Control bit1, when CHANCTRL:Interrupt Disable for that channel is reset).

6.5.8 cs_status

Chipset Status.

Type: MEM Bus: 0 Offset: 0xe	PortID: 8'h7e Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
3:3	RO	0x0	address_remapping: This bit reflects the TE bit of the non-VC1 Intel VT-d engine
2:2	RO	0x0	memory_bypass:
1:1	RO	0x0	mmio_restriction:

6.5.9 dmacapability

Type: MEM Bus: 0 Offset: 0x10		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
9:9	RO_V (Function 0-1) RO (Function 2-7)	0x0	xor_raid6: If set, specifies XOR with Galios Field Multiply Parity and Quotient opcodes for RAID5 and RAID6 are supported. The opcodes are: 0x89 - XOR with Galios Field Multiply Generation 0x8A - XOR with Galios Field Multiply Validate 0x8B - XOR with Galios Field Multiply Update Generation Notes: When this bit is zero, the DMA engine will halt if it encounters a descriptor with these opcodes.
8:8	RO	0x0	xor_raid5: If set, specifies XOR without Galios Field Multiply parity only opcodes for RAID5 are supported. The opcodes are: 0x87 - XOR Generation 0x88 - XOR Validate Notes: When this bit is zero, the DMA engine will halt if it encounters a descriptor with these opcodes.
7:7	RO	0x1	extended_apic_id: Set if 32b APIC ID's are supported. 1: 32b APIC ID's supported 0: 8b APIC ID's supported
6:6	RO	0x1	block_fill: If set, specifies the Block Fill opcode is supported. The opcode is: 0x01 - Block Fill Notes: When this bit is zero, the DMA engine will abort if it encounters a descriptor with these opcodes.
5:5	RO	0x1	move_crc: If set, specifies Move and CRC opcodes are supported. The opcodes are: 0x41 - Move and Generate CRC-32 0x42 - Move and Test CRC-32 0x43 - Move and Store CRC-32 Notes: When this bit is zero, the DMA engine will abort if it encounters a descriptor with these opcodes.
4:4	RW_O	0x1	dca: If set, specifies DMA DCA operations are supported according to the settings in the descriptors. Notes: When this bit is zero, the DMA engine ignores the DCA hints in DMA descriptors. This bit is RW-O to give bios the ability to turn off DCA operation from Intel QuickData Technology DMA.
3:3	RO	0x0	xor: If set, specifies XOR opcodes are supported. Opcodes are: 0x85 - original XOR Generation 0x86 - original XOR Validate Notes: These opcodes have been deprecated in Intel QuickData Technology DMA v3. The DMA engine will abort if it encounters a descriptor with these opcodes.

Type: MEM Bus: 0 Offset: 0x10		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
2:2	RO	0x1	marker_skipping: If set, specifies the Marker Skipping opcode is supported. The opcode is: 0x84 - Marker Skipping Notes: When this bit is zero, the DMA engine will abort if it encounters a descriptor with this opcode.
1:1	RO	0x1	crc: If set, specifies CRC Generation opcodes are supported. Opcodes are: 0x81 - CRC-32 Generation 0x82 - CRC-32 Generation & Test 0x83 - CRC-32 Generation & Store Notes: When this bit is zero, the DMA engine will abort if it encounters a descriptor with these opcodes.
0:0	RO	0x1	page_break: If set, specifies a transfer crossing physical pages is supported. Notes: When this bit is zero, software must not set SPBrk nor DPBrk bits in the DMA descriptor and the DMA engine generates an error if either of those bits are set

6.5.10 dcaoffset

Type: MEM Bus: 0 Offset: 0x14		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x100	dcaregptr:

6.5.11 cbprio

Intel QuickData Technology DMA Priority Register.

Type: MEM Bus: 0 Offset: 0x40		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	not_used:

6.5.12 chanctrl

The Channel Control register controls the behavior of the DMA channel when specific events occur such as completion or errors.

Type: MEM Bus: 0 Offset: 0x80		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
9:9	RW_L	0x0	cmpwr_dca_enable: When this bit is set, and the DMA engine supports DCA, then completion writes will be directed to the CPU indicated in Target CPU.This field is RW if CHANCNT register is 1 otherwise this register is RO.
8:8	RW_LV	0x0	in_use: In Use. This bit indicates whether the DMA channel is in use. The first time this bit is read after it has been cleared, it will return 0 and automatically transition from 0 to 1, reserving the channel for the first consumer that reads this register. All subsequent reads will return 1 indicating that the channel is in use. This bit is cleared by writing a 0 value, thus releasing the channel. A consumer uses this mechanism to atomically claim exclusive ownership of the DMA channel. This should be done before attempting to program any register in the DMA channel register set. This field is RW if CHANCNT register is 1 otherwise this register is RO.
5:5	RW_L	0x0	desc_addr_snp_ctrl: Descriptor address snoop control. 1: When set, this bit indicates that the descriptors are not in coherent space and should not be snooped. 0: When cleared, the descriptors are in coherent space and each descriptor address must be snooped on QPI. This field is RW if CHANCNT register is 1 otherwise this register is RO.
4:4	RW_L	0x0	err_int_en: Error Interrupt Enable. This bit enables the DMA channel to generate an interrupt (MSI or legacy) when an error occurs during the DMA transfer. If Any Error Abort Enable (see below) is not set, then unaffiliated errors do not cause an interrupt.This field is RW if CHANCNT register is 1 otherwise this register is RO.
3:3	RW_L	0x0	anyerr_abrt_en: Any Error Abort Enable. This bit enables an abort operation when any error is encountered during the DMA transfer. When the abort occurs, the DMA channel generates an interrupt and a completion update as per the Error Interrupt Enable and Error Completion Enable bits. When this bit is reset, only affiliated errors cause the DMA channel to abort.This field is RW if CHANCNT register is 1 otherwise this register is RO.
2:2	RW_L	0x0	err_cmp_en: Error Completion Enable. This bit enables a completion write to the address specified in the CHANCMP register upon encountering an error during the DMA transfer. If Any Error Abort is not set, then unaffiliated errors do not cause a completion write.This field is RW if CHANCNT register is 1 otherwise this register is RO.
0:0	RW1C	0x0	intp_dis: Interrupt Disable. Upon completing a descriptor, if an interrupt is specified for that descriptor and this bit is reset, then the DMA channel generates an interrupt and sets this bit. The choice between MSI or legacy interrupt mode is determined with the MSICTRL register. Legacy interrupts are further gated through intxDisable in thePCICMD register of the Intel QuickData Technology DMA PCI configuration space. The controlling process can re-enable this channel's interrupt by writing a one to this bit, which clears the bit. Writing a zero has no effect. Thus, each time this bit is reset, it enables the DMA channel to generate one interrupt.

6.5.13 dma_comp

DMA Compatibility Register.

Type: MEM Bus: 0 Offset: 0x82		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
2:2	RO	0x1	v3_compatibility: Compatible with version 3 Intel QuickData Technology spec
1:1	RO	0x1	v2_compatibility: Compatible with version 2 Intel QuickData Technology spec
0:0	RO	0x0	v1_compatibility: Not compatible with version 1

6.5.14 chancmd

DMA Channel Command Register.

Setting more than one of these bits with the same write operation will result in an Fatal error affiliated.

Type: MEM Bus: 0 Offset: 0x84		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
5:5	RW_LV	0x0	reset_dma: Set this bit to reset the DMA channel. Setting this bit is a last resort to recover the DMA channel from a programming error or other problem such as dead lock from cache coherency protocol. Execution of this command does not generate an interrupt or generate status. This command causes the DMA channel to return to a known state Halted.This field is RW if CHANCNT register is 1 otherwise this register is RO.
2:2	RW_LV	0x0	susp_dma: Suspend DMA. Set this bit to suspend the current DMA transfer. This field is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.15 dmacount

DMA Descriptor Count Register.

Type: MEM Bus: 0 Offset: 0x86		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RW_L	0x0	numdesc: This is the absolute value of the number of valid descriptors in the chain. The hardware sets this register and an internal counter to zero whenever the CHAINADDR register is written. When this register does not equal the value of the internal register, the DMA channel processes descriptors, incrementing the internal counter each time that it completes (or skips) a descriptor.This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.16 chansts_0

Channel Status 0 Register.

The Channel Status Register records the address of the last descriptor completed by the DMA channel.

Type: MEM Bus: 0 Offset: 0x88		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:6	RO	0x0	cmpdscaddr: This register stores the upper address bits (64B aligned) of the last descriptor processed. The DMA channel automatically updates this register when an error or successful completion occurs. For each completion, the DMA channel over-writes the previous value regardless of whether that value has been read.
2:0	RO	0x3	dma_trans_state: DMA Transfer Status. The DMA engine sets these bits indicating the state of the current DMA transfer. The cause of an abort can be either error during the DMA transfer or invoked by the controlling process via the CHANCMD register.000 - Active 001 - Idle, DMA Transfer Done (no hard errors) 010 - Suspended 011 - Halted, operation aborted 100 - Armed

6.5.17 chansts_1

Channel Status 1 Register.

The Channel Status Register records the address of the last descriptor completed by the DMA channel.

Type: MEM Bus: 0 Offset: 0x8c		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RO	0x0	cmpdscaddr: This register stores the upper address bits (64B aligned) of the last descriptor processed. The DMA channel automatically updates this register when an error or successful completion occurs. For each completion, the DMA channel over-writes the previous value regardless of whether that value has been read.

6.5.18 chainaddr_0

Descriptor Chain Address 0 Register.

This register is written by the processor to specify the first descriptor to be fetched by the DMA channel.

Type: MEM Bus: 0 Offset: 0x90	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
31:0	RW_L	0x0	dscaddrlo: This 64 bit field marks the address of the first descriptor to be fetched by the DMA channel. The least significant 6 bits must be zero for the address to be valid. This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.19 chainaddr_1

Descriptor Chain Address 1 Register.

This register is written by the processor to specify the first descriptor to be fetched by the DMA channel.

Type: MEM Bus: 0 Offset: 0x94	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
31:0	RW_L	0x0	dscaddrhi: This 64 bit field marks the address of the first descriptor to be fetched by the DMA channel. The least significant 6 bits must be zero for the address to be valid. This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.20 chancmp_0

Channel Completion Address 0 Register.

This register specifies the address where the DMA channel writes the completion status upon completion or an error condition i.e. it writes the contents of the CHANSTS register to the destination as pointed by the CHANCMP register.

Type: MEM Bus: 0 Offset: 0x98	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
31:3	RW_L	0x0	chcmpladdr_lo: This 64-bit field specifies the address where the DMA engine writes the completion status (CHANSTS). This address can fall within system memory or memory-mapped I/O space but should be 8-byte aligned.This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.21 chancmp_1

Channel Completion Address 1 Register.

This register specifies the address where the DMA channel writes the completion status upon completion or an error condition i.e. it writes the contents of the CHANSTS register to the destination as pointed by the CHANCMP register.

Type: MEM **Bus:** 0 **Offset:** 0x9c	**PortID:** 8'h7e **Device:** 4	**Function:** 0-7	
Bit	**Attr**	**Default**	**Description**
31:0	RW_L	0x0	chcmpladdr_hi: This 64-bit field specifies the address where the DMA engine writes the completion status (CHANSTS). This address can fall within system memory or memory-mapped I/O space but should be 8-byte aligned.This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.22 chanerr

The Channel Error Register records the error conditions occurring within a given DMA channel.

Type: MEM **Bus:** 0 **Offset:** 0xa8	**PortID:** 8'h7e **Device:** 4	**Function:** 0-7	
Bit	**Attr**	**Default**	**Description**
18:18	RW1CS (Function 0-1) RO (Function 2-7)	0x0	desccnterr: The hardware sets this bit when it encounters a base descriptor that requires an extended descriptor (such as an XOR with 8 sources), but DMACount indicates that the Base descriptor is the last descriptor that can be processed.
17:17	RW1CS (Function 0-1) RO (Function 2-7)	0x0	xorqerr: The hardware sets this bit when the Q validation part of the XOR with Galois Field Multiply Validate operation fails.
16:16	RW1CS	0x0	crc_xorp_err: The hardware sets this bit when a CRC Test operation or XOR Validity operation fails or when the P validation part of the XOR with Galois Field Multiply Validate operation fails.
15:15	RO	0x0	unaffil_err: Unaffiliated Error . IIO never sets this bit
13:13	RW1CS	0x0	int_cfg_err: Interrupt Configuration Error. The DMA channel sets this bit indicating that the interrupt registers were not configured properly when the DMA channel attempted to generate an interrupt. E.g. interrupt address is not 0xFEE.
12:12	RW1CS	0x0	cmp_addr_err: Completion Address Error. The DMA channel sets this bit indicating that the completion address register was configured to an illegal address or has not been configured.
11:11	RW1CS	0x0	desc_len_err: Descriptor Length Error. The DMA channel sets this bit indicating that the current transfer has an illegal length field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.

Type: MEM Bus: 0 Offset: 0xa8	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
10:10	RW1CS	0x0	desc_ctrl_err: Descriptor Control Error. The DMA channel sets this bit indicating that the current transfer has an illegal control field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
9:9	RW1CS	0x0	wr_data_err: Write Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while writing the destination data. This error could be because of an internal ram error in the write queue that stores the write data before being written to main memory. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
8:8	RW1CS	0x0	rd_data_err: Read Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while accessing the source data. This error could be a read data that is received poisoned. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
7:7	RW1CS	0x0	dma_data_parerr: DMA Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered an uncorrectable ECC/parity error reported by the DMA engine.
6:6	RW1CS	0x0	cdata_parerr: Chipset Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered a parity error reported by the chipset. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
5:5	RW1CS	0x0	chancmd_err: CHANCMD Error. The DMA channel sets this bit indicating that a write to the CHANCMD register contained an invalid value (for example. more than one command bit set).
4:4	RW1CS	0x0	chn_addr_valerr: Chain Address Value Error. The DMA channel sets this bit indicating that the CHAINADDR register has an illegal address including an alignment error (not on a 64-byte boundary).
3:3	RW1CS	0x0	descriptor_error: The DMA channel sets this bit indicating that the current transfer has encountered an error (not otherwise covered under other error bits) when reading or executing a DMA descriptor. When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
2:2	RW1CS	0x0	nxt_desc_addr_err: Next Descriptor Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal next descriptor address including an alignment error (not on a 64-byte boundary). When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
1:1	RW1CS	0x0	dma_xfrer_daddr_err: DMA Transfer Destination Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal destination address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.

Type: MEM Bus: 0 Offset: 0xa8	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
0:0	RW1CS	0x0	dma_trans_saddr_err: DMA Transfer Source Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal source address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.

6.5.23 chanerrmsk

Channel Error Mask Register.

Type: MEM Bus: 0 Offset: 0xac	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
18:18	RWS (Function 0-1) RO (Function 2-7)	0x0	mask18: This register is a bit for bit mask for the CHANERR register 0: enable 1: disable
17:17	RWS (Function 0-1) RO (Function 2-7)	0x0	mask17: This register is a bit for bit mask for the CHANERR register 0: enable 1: disable
16:16	RWS	0x0	mask16: This register is a bit for bit mask for the CHANERR register 0: enable 1: disable
13:0	RWS	0x0	mask13_0: This register is a bit for bit mask for the CHANERR register 0: enable 1: disable

6.5.24 dcactrl

DCA Control.

Type: MEM Bus: 0 Offset: 0xb0	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
15:0	RW_L	0x0	target_cpu: Specifies the APIC ID of the target CPU for Completion Writes. This field is RW if CHANCNT register is 1 otherwise this register is RO.

6.5.25 dca_ver

DCA Version Number Register.

Type: MEM Bus: 0 Offset: 0x100		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:4	RO	0x1	major_revision:
3:0	RO	0x0	minor_revision:

6.5.26 dca_reqid_offset

DCA Requester ID Offset.

Type: MEM Bus: 0 Offset: 0x102		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x180	dca_reqid_regs: registers are at offset 180h

6.5.27 csi_capability

Intel QPI Compatibility Register.

Type: MEM Bus: 0 Offset: 0x108		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RO	0x1	prefetch_hint: IIO supports Prefetch Hint only method on the coherent interface

6.5.28 pcie_capability

PCI Express Capability Register.

Type: MEM Bus: 0 Offset: 0x10a		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RO	0x1	memwr: IIO supports only memory write method on PCI Express

6.5.29 csi_cap_enable

Intel QPI Capability Enable Register.

Type: MEM Bus: 0 Offset: 0x10c	PortID: 8’h7e Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x0	enable_prefetch_hint: When set in function 0, DCA on Intel QPI is enabled, else disabled. IIO hardware does not use this bit from functions 1-7. In these functions, this bit is provided primarily for BIOS to communicate to driver that DCA is enabled in the IIO.

6.5.30 pcie_cap_enable

PCI Express Capability Enable Register.

Type: MEM Bus: 0 Offset: 0x10e	PortID: 8’h7e Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x0	enable_memwr_on_pcie: When set in function 0, DCA on PCIe is enabled, else disabled. IIO hardware does not use this bit from functions 1-7. In these functions, this bit is provided primarily for BIOS to communicate to driver that DCA is enabled in the IIO.

6.5.31 apicid_tag_map

APICID to Tag Map Register.

When DCA is disabled, DMA engine uses all 1s in the tag field of the write.

This register is setup by BIOS for the Intel QuickData Technology driver to read. BIOS will map APICID[7:5] to bits Tag[2:0]. BIOS should set Tag[4] to prevent implicit TPH cache target unless it is intended.

Type: MEM Bus: 0 Offset: 0x110	PortID: 8’h7e Device: 4		Function: 0-7
Bit	**Attr**	**Default**	**Description**
39:32	RW	0x80	tag_map_4: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 4 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[4] = Tag_Map_4[0] 01: Tag[4] = APICID[Tag_Map_4[3:0]] 10: Tag[4] = NOT(APICID [Tag_Map_4[3:0]]) 11: reserved

Type: MEM Bus: 0 Offset: 0x110	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
31:24	RW	0x80	tag_map_3: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 3 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[3] = Tag_Map_3[0] 01: Tag[3] = APICID[Tag_Map_3[3:0]] 10: Tag[3] = NOT(APICID[Tag_Map_3[3:0]]) 11: reserved
23:16	RW	0x80	tag_map_2: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 2 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[2] = Tag_Map_2[0] 01: Tag[2] = APICID[Tag_Map_2[3:0]] 10: Tag[2] = NOT(APICID[Tag_Map_2[3:0]]) 11: reserved
15:8	RW	0x80	tag_map_1: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 1 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[1] = Tag_Map_1[0] 01: Tag[1] = APICID[Tag_Map_1[3:0]] 10: Tag[1] = NOT(APICID[Tag_Map_1[3:0]]) 11: reserved
7:0	RW	0x80	tag_map_0: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 0 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[0] = Tag_Map_0[0] 01: Tag[0] = APICID[Tag_Map_0[3:0]] 10: Tag[0] = NOT (APICID[Tag_Map_0[3:0]]) 11: reserved

6.5.32 dca_reqid[0:1]

Global DCA Requester ID Table Registers.

Type: MEM Bus: 0 Offset: 0x180, 0x184	PortID: 8'h7e Device: 4	Function: 0-7	
Bit	**Attr**	**Default**	**Description**
31:31	RO	0x0	last: This bit is set only in the last RequesterID register for this port. Thus, it identifies that this is the last DCA RequesterID register for this port.
29:29	RW	0x0	valid: when set the requester id programed into bits 15:0 is used by hardware for DCA write identification, otherwise the bits are ignored.

Type: MEM Bus: 0 Offset: 0x180, 0x184		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
28:28	RW	0x0	ignore_function_number: When set, the function number field in the RequesterID is ignored when authenticating a DCA write, otherwise the function number is included
15:8	RW	0x0	bus_number: PCI bus number of the DCA requester
7:3	RW	0x0	device_number: Device number of the day requester
2:0	RW	0x0	function_number: Function number of the day requester

6.5.33 msgaddr

MSI-X Lower Address Registers.

Type: MEM Bus: 0 Offset: 0x2000		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:2	RW_V	0x0	chmsgaddr: Specifies the local APIC to which this MSI-X interrupt needs to be sent.
1:0	RO	0x0	chmsgaddr_const:

6.5.34 msgupaddr

MSI-X Upper Address Registers.

Type: MEM Bus: 0 Offset: 0x2004		PortID: 8’h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RW_V	0x0	chmsgupaddr_const: Reserved to 0 because does not apply to IA. This field is RW for compatibility reason only.

6.5.35 msgdata

MSI-X Data Registers.

Type: MEM Bus: 0 Offset: 0x2008		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RW_V	0x0	chmsgdata: Specifies the vector that needs to be used for interrupts from the DMA engine. IIO uses the lower 16 bits of this field to form the data portion of the interrupt on the coherent interface. The upper 16 bits are not used by IIO and left as RW only for compatibility reasons.

6.5.36 vecctrl

MSI-X Vector Control Registers.

Type: MEM Bus: 0 Offset: 0x200c		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:1	RO	0x0	chvecctrlcnst:
0:0	RW_V	0x1	chmask: When a bit is set, the channel is prohibited from sending a message, even if all other internal conditions for interrupt generation are valid.

6.5.37 pendingbits

MSI-X Interrupt Pending Bits Registers.

Type: MEM Bus: 0 Offset: 0x3000		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
31:1	RO	0x0	chmsipendcnst: unused
0:0	RW_V	0x0	chmsipend: Pending Bit (when set) indicates that the DMA engine has a pending MSI-X message for the DMA Channel. This bit is cleared by hardware as soon as it issues the MSI-X message. Note that a Pending Bit is set only if all internal conditions for generation of an MSIX interrupt (like the Channel Interrupt Disable bit being cleared, etc.) are valid. This does not include the MSI-X Mask bit for the channel and the MSI-X Function Mask bit. Once set, a Pending Bit remains set until: The corresponding MSI-X Mask bit and the MSI-X Function Mask bit are both cleared, at which time the IIO issues the pending message and clears the bit. Pending bit is cleared when the Interrupt Disable bit in the corresponding 'Channel Control Register (CHANCTRL)' transitions from 1b to 0b and there is not another interrupt pending for that channel - no MSI-X message issued. Implementation Note: Implementations can consider an MSI message 'issued to the system', as soon as the message is 'posted' internally in the device.

6.6 Device 5 Function 0

Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d), Address Mapping, System Management, Coherent Interface, Misc Registers.

Register Name	Offset	Size
vid	0x0	16
did	0x2	16
pcicmd	0x4	16
pcists	0x6	16
rid	0x8	8
ccr	0x9	24
clsr	0xc	8
hdr	0xe	8
svid	0x2c	16
sdid	0x2e	16
capptr	0x34	8
intl	0x3c	8
intpin	0x3d	8
pxpcapid	0x40	8
pxpnxtptr	0x41	8
pxpcap	0x42	16
hdrtypectrl	0x80	8
mmcfg_base	0x90	64
mmcfg_limit	0x98	64
tommiol_ob	0xa4	32
tseg	0xa8	64
genprotrange1_base	0xb0	64
genprotrange1_limit	0xb8	64
genprotrange2_base	0xc0	64
genprotrange2_limit	0xc8	64
tolm	0xd0	32
tohm	0xd4	64
tommiol	0xdc	32
ncmem_base	0xe0	64
ncmem_limit	0xe8	64
mencmem_base	0xf0	64
mencmem_limit	0xf8	64
cpubusno	0x108	32
lmmiol_base	0x10c	16
lmmiol_limit	0x10e	16
lmmioh_base	0x110	64
lmmioh_limit	0x118	64
genprotrange0_base	0x120	64
genprotrange0_limit	0x128	64

Register Name	Offset	Size
gcfgbus_base	0x134	8
gcfgbus_limit	0x135	8
cipctrl	0x140	32
cipsts	0x144	32
cipdcasad	0x148	32
cipintrc	0x14c	64
cipintrs	0x154	32
vtbar	0x180	32
vtgenctrl	0x184	16
vtisochctrl	0x188	32
vtgenctrl2	0x18c	32
iotlbpartition	0x194	32
vtuncerrsts	0x1a8	32
vtuncerrmsk	0x1ac	32
vtuncerrsev	0x1b0	32
vtuncerrptr	0x1b4	8
iiomiscctrl	0x1c0	64
ltdpr	0x290	32
lcfgbus_base	0x41c	8
lcfgbus_limit	0x41d	8
csipintrs	0x450	32

6.6.1 vid

Type: CFG **PortID:** N/A
Bus: 0 **Device:** 5 **Function:** 0
Offset: 0x0

Bit	Attr	Default	Description
15:0	RO	0x8086	vendor_identification_number: The value is assigned by PCI-SIG to Intel.

6.6.2 did

Type: CFG **PortID:** N/A
Bus: 0 **Device:** 5 **Function:** 0
Offset: 0x2

Bit	Attr	Default	Description
15:0	RO	0x2f28	device_identification_number: Device ID values vary from function to function.

6.6.3 pcicmd

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 0
Offset: 0x4		

Bit	Attr	Default	Description
10:10	RO	0x0	intx_disable: NA for these devices
9:9	RO	0x0	fast_back_to_back_enable: Not applicable to PCI Express and is hardwired to 0
8:8	RO	0x0	serr_enable: This bit has no impact on error reporting from these devices
7:7	RO	0x0	idsel_stepping_wait_cycle_control: Not applicable to internal devices. Hardwired to 0.
6:6	RO	0x0	parity_error_response: This bit has no impact on error reporting from these devices
5:5	RO	0x0	vga_palette_snoop_enable: Not applicable to internal devices. Hardwired to 0.
4:4	RO	0x0	memory_write_and_invalidate_enable: Not applicable to internal devices. Hardwired to 0.
3:3	RO	0x0	special_cycle_enable: Not applicable. Hardwired to 0.
2:2	RO	0x0	bus_master_enable: Hardwired to 0 since these devices don't generate any transactions
1:1	RO	0x0	memory_space_enable: Hardwired to 0 since these devices don't decode any memory BARs
0:0	RO	0x0	io_space_enable: Hardwired to 0 since these devices don't decode any IO BARs

6.6.4 pcists

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 0
Offset: 0x6		

Bit	Attr	Default	Description
15:15	RO	0x0	detected_parity_error: This bit is set when the device receives a packet on the primary side with an uncorrectable data error including a packet with poison bit set or an uncorrectable addresscontrol parity error. The setting of this bit is regardless of the Parity Error Response bit PERRE in the PCICMD register. IIO will never set this bit.
14:14	RO	0x0	signaled_system_error: Hardwired to 0
13:13	RO	0x0	received_master_abort: Hardwired to 0
12:12	RO	0x0	received_target_abort: Hardwired to 0
11:11	RO	0x0	signaled_target_abort: Hardwired to 0
10:9	RO	0x0	devsel_timing: Not applicable to PCI Express. Hardwired to 0.

Type: CFG Bus: 0 Offset: 0x6		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
8:8	RO	0x0	master_data_parity_error: Hardwired to 0
7:7	RO	0x0	fast_back_to_back: Not applicable to PCI Express. Hardwired to 0.
5:5	RO	0x0	pci66mhz_capable: Not applicable to PCI Express. Hardwired to 0.
4:4	RO	0x1	capabilities_list: This bit indicates the presence of a capabilities list structure
3:3	RO	0x0	intx_status: Hardwired to 0

6.6.5 rid

Type: CFG Bus: 0 Offset: 0x8		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register in any Intel® Xeon® Processor E7 v4 product family function.

6.6.6 ccr

Type: CFG Bus: 0 Offset: 0x9		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
23:16	RO_V	0x8	base_class: Generic Device
15:8	RO_V	0x80	sub_class: Generic Device
7:0	RO_V	0x0	register_level_programming_interface: Set to 00h for all non-APIC devices.

6.6.7 clsr

Type: CFG Bus: 0 Offset: 0xc		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	cacheline_size: This register is set as RW for compatibility reasons only. Cacheline size is always 64B.

6.6.8 hdr

Type: CFG Bus: 0 Offset: 0xe		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:7	RO	0x1	multi_function_device: This bit defaults to 1b since all these devices are multi-function
6:0	RO	0x0	configuration_layout: This field identifies the format of the configuration header layout. It is Type 0 for all these devices. The default is 00h, indicating a 'endpoint device'.

6.6.9 svid

Type: CFG Bus: 0 Offset: 0x2c		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x0	subsystem_vendor_identification_number: The default value specifies Intel but can be set to any value once after reset.

6.6.10 sdid

Type: CFG Bus: 0 Offset: 0x2e		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x0	subsystem_device_identification_number: Assigned by the subsystem vendor to uniquely identify the subsystem

6.6.11 capptr

Type: CFG Bus: 0 Offset: 0x34		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x40	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.

6.6.12 intl

Type: CFG Bus: 0 Offset: 0x3c		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	interrupt_line: NA for these devices

6.6.13 intpin

Type: CFG Bus: 0 Offset: 0x3d		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	interrupt_pin: NA since these devices do not generate any interrupt on their own

6.6.14 pxpcapid

Type: CFG Bus: 0 Offset: 0x40		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x10	capability_id: Provides the PCI Express capability ID assigned by PCI-SIG.

6.6.15 pxpnxtptr

Type: CFG Bus: 0 Offset: 0x41		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	next_ptr: This field is set to the PCI Power Management capability.

6.6.16 pxpcap

Type: CFG Bus: 0 Offset: 0x42		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
13:9	RO	0x0	interrupt_message_number_n_a:
8:8	RO	0x0	slot_implemented_n_a:
7:4	RO	0x9	device_port_type: This field identifies the type of device. It is set to for the DMA to indicate root complex integrated endpoint device.
3:0	RO	0x2	capability_version: This field identifies the version of the PCI Express capability structure. Set to 2h for PCI Express and DMA devices for compliance with the extended base registers.

6.6.17 hdrtypectrl

PCI Header Type Control

Type: CFG Bus: 0 Offset: 0x80		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
2:0	RW	0x0	clr_hdrmfd: When set, function#0 with in the indicated device shows a value of 0 for bit 7 of the HDR register, indicating a single function device. BIOS sets this bit, when only function#0 is visible within the device, either because SKU reasons or BIOS has hidden all functions but function#0 within the device via the DEVHIDE register. Bit 0 is for Device#1 Bit 1 is for Device#2 Bit 3 is for Device#3 Currently this is defined only for devices 1, 2 and 3 because in other devices it is expected that at least 2 functions are visible to OS or the entire device is hidden.

6.6.18 mmcfg_base

MMCFG Address Base

Type: CFG Bus: 0 Offset: 0x90		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:26	RW_LB	0x3f	mmcfg_base_addr: Indicates the base address which is aligned to a 64 MB boundary.

6.6.19 mmcfg_limit

MMCFG Address Limit.

Type: CFG Bus: 0 Offset: 0x98		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:26	RW_LB	0x0	mmcfg_limit_addr: Indicates the limit address which is aligned to a 64MB boundary. Any access that decodes to be between MMCFG.BASE<= Addr <= MMCFG.LIMIT targets the MMCFG region and is aborted by IIO. Setting the MMCFG.BASE greater than MMCFG.LIMIT, disables this region.

6.6.20 tommiol_ob

Type: CFG Bus: 0 Offset: 0xA4		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:20	RW_LB	0x0FBF	tommiol_ob: This field is used to prevent non-DMI links, along with Intel QuickData Technology/APIC primary BARs, from claiming outbound addresses starting above this address and ending at 0xffff_ffff. Bits 19:0 are zero and not writable, and are treated as 1's (like TOLM and TOHM). Set this to 0xfff to disable TOMMIOL_OB. This is intended to be set consistently with TOMMIOL, but the two can be different if needed.

6.6.21 tseg

Type: CFG Bus: 0 Offset: 0xa8		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:52	RW_LB	0x0	limit: Indicates the limit address which is aligned to a 1MB boundary. Any access to falls within TSEG.BASE[31:20] <= Addr[31:20] <= TSEG.LIMIT[31:20] is considered to target the Tseg region and IIO aborts it. Note that address bits 19:0 are ignored and not compared. The result is that BASE[19:0] is effectively 00000h and LIMIT is effectively FFFFFh. Setting the TSEG.BASE greater than the limit, disable this region.
31:20	RW_LB	0xfe0	base: Indicates the base address which is aligned to a 1MB boundary. Bits [31:20] corresponds to A[31:20] address bits.

6.6.22 genprotrange[1:0]_base

Generic Protected Memory Range X Base Address. (X = 1, 0)

Type: CFG Bus: 0 Offset: 0xb0, 0x120		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
50:16	RW_LB	0x7fffffff	base_address: [50:16] of generic memory address range that needs to be protected from inbound dma accesses. The protected memory range can be anywhere in the memory space addressable by the processor. Addresses that fall in this range i.e. GenProtRange.Base[63:16] <= Address [63:16] <= GenProtRange.Limit [63:16], are completer aborted by IIO. Setting the Protected range base address greater than the limit address disables the protected memory region. Note that this range is orthogonal to Intel VT-d spec defined protected address range. Since this register provides for a generic range, it can be used to protect any system dram region or MMIO region from DMA accesses. But the expected usage for this range is to abort all PCIe accesses to the PCI-Segments region.

6.6.23 genprotrange[1:0]_limit

Generic Protected Memory Range X Limit Address. (X = 1, 0)

Type: CFG Bus: 0 Offset: 0xb8, 0x128		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RW_LB	0x0	limit_address: [50:16] of generic memory address range that needs to be protected from inbound dma accesses. The protected memory range can be anywhere in the memory space addressable by the processor. Addresses that fall in this range i.e. GenProtRange.Base[63:16] <= Address [63:16] <= GenProtRange.Limit [63:16], are completer aborted by IIO. Setting the Protected range base address greater than the limit address disables the protected memory region. Note that this range is orthogonal to Intel VT-d spec defined protected address range. This register is programmed once at boot time and does not change after that, including any quiesce flows. Since this register provides for a generic range, it can be used to protect any system dram region from DMA accesses. The expected usage for this range is to abort all PCIe accesses to the PCI-Segments region.

6.6.24 genprotrange2_base

Generic Protected Memory Range 2 Base Address.

Type: CFG Bus: 0 Offset: 0xc0		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
50:16	RW_LB	0x7fffffff	base_address: [50:16] of generic memory address range that needs to be protected from inbound dma accesses. The protected memory range can be anywhere in the memory space addressable by the processor. Addresses that fall in this range i.e. GenProtRange.Base[63:16] <= Address [63:16] <= GenProtRange.Limit [63:16], are completer aborted by IIO. Setting the Protected range base address greater than the limit address disables the protected memory region. Note that this range is orthogonal to Intel VT-d spec defined protected address range. This register is programmed once at boot time and does not change after that, including any quiesce flows. This region is expected to be used to protect against PAM region accesses inbound, but could also be used for other purposes, if needed.

6.6.25 genprotrange2_limit

Generic Protected Memory Range 2 Limit Address.

Type: CFG Bus: 0 Offset: 0xc8		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RW_LB	0x0	limit_address: [50:16] of generic memory address range that needs to be protected from inbound dma accesses. The protected memory range can be anywhere in the memory space addressable by the processor. Addresses that fall in this range i.e. GenProtRange.Base[63:16] <= Address [63:16] <= GenProtRange. Limit [63:16], are completer aborted by IIO. Setting the Protected range base address greater than the limit address disables the protected memory region. Note that this range is orthogonal to Intel VT-d spec defined protected address range. This register is programmed once at boot time and does not change after that, including any quiesce flows. This region is expected to be used to protect against PAM region accesses inbound, but could also be used for other purposes, if needed.

6.6.26 tolm

Top of Low Memory

Type: CFG Bus: 0 Offset: 0xd0	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
31:26	RW_LB	0x0	addr: TOLM Address. Indicates the top of low dram memory which is aligned to a 64MB boundary. A 32 bit transaction that satisfies '0 <= Address[31:26] <= TOLM[31:26]' is a transaction towards main memory.

6.6.27 tohm

Top of High Memory.

Type: CFG Bus: 0 Offset: 0xd4	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
63:26	RW_LB	0x0	addr: TOHM Address. Indicates the limit of an aligned 64 MB granular region that decodes >4 GB addresses towards system dram memory. A 64-bit transaction that satisfies '4G <= A[63:26] <= TOHM[63:26]' is a transaction towards main memory. This register is programmed once at boot time and does not change after that, including during quiesce flows.

6.6.28 tommiol

Type: CFG Bus: 0 Offset: 0xdc	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
31:20	RW_LB	0x0FBF	tommiol: This field is used to abort inbound MRd/MWr/atomic accesses starting above this address and ending at 0xffff_ffff, exclusive of the interrupt hole (0xfeex_xxxx). Bits 19:0 are zero and not writable, and are treated as 1's (like TOLM and TOHM). Set this to 0xfff to disable TOMMIOL.

6.6.29 ncmem_base

Non-Coherent Memory Base Address.

Type: CFG Bus: 0 Offset: 0xe0		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:26	RW_LB	0x3fffffff	addr: Non Coherent memory base address. Describes the base address of a 64MB aligned dram memory region on Intel QPI that is non-coherent. Address bits [63:26] of an inbound address if it satisfies 'NcMem.Base[63:26] <= A[63:26] <= NcMem.Limit[63:26]' is considered to be towards the non-coherent Intel QPI memory region. The range indicated by the Non-coherent memory base and limit registers does not necessarily fall within the low dram or high dram memory regions as described via the corresponding base and limit registers. This register is programmed once at boot time and does not change after that, including any quiesce flows

6.6.30 ncmem_limit

Non-Coherent Memory Limit.

Type: CFG Bus: 0 Offset: 0xe8		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:26	RW_LB	0x0	addr: Non Coherent memory limit address. Describes the limit address of a 64 MB aligned dram memory region on Intel QPI that is non-coherent. Address bits [63:26] of an inbound address if it satisfies 'NcMem.Base[63:26] <= A[63:26] <= NcMem.Limit[63:26]' is considered to be towards the non-coherent Intel QPI memory region. The range indicated by the Non-coherent memory base and limit registers does not necessarily fall within the low dram or high dram memory regions as described via the corresponding base and limit registers. This register is programmed once at boot time and does not change after that, including any quiesce flows.

6.6.31 mencmem_base

Intel® Management Engine (Intel® ME) Non-Coherent Memory Base Address.

Type: CFG Bus: 0 Offset: 0xf0		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:19	RW_LB	0x1fffffffff	addr: Intel® Management Engine (Intel® ME) UMA Base Address. Indicates the base address which is aligned to a 1MB boundary. Bits [63:19] corresponds to A[63:19] address bits.

6.6.32 mencmem_limit

Intel® Management Engine (Intel® ME) Non-Coherent Memory Base Limit.

Type: CFG Bus: 0 Offset: 0xf8	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
63:19	RW_LB	0x0	addr: Intel ME UMA Limit Address. Indicates the limit address which is aligned to a 1MB boundary. Bits [63:19] corresponds to A[63:19] address bits.Any address that falls within MENCMEMBASE <= Addr <= MENCMEMLIMIT range is considered to target the UMA range. Setting the MCNCMEMBASE greater than the MCNCMEMLIMIT disables this range. The range indicated by this register must fall within the low dram or high dram memory regions as described via the corresponding base and limit registers.

6.6.33 cpubusno

CPU Internal Bus Numbers.

Type: CFG Bus: 0 Offset: 0x108	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
24:17	RW_LB	0x0	segment:
16:16	RW_LB	0x0	valid: 1: IIO claims PCI config accesses if: the bus# matches the value in bits 7:0 of this register and Dev# >= 16 OR the bus# does not match either the value in bits 7:0 or 15:8 of this register 0: IIO does not claim PCI config accesses
15:8	RW_LB	0x0	bus1: Is the internal bus# of rest of uncore (not including IIO). All devices are claimed on behalf of this component. Devices that do not exist within this component on this bus number are master aborted.
7:0	RW_LB	0x0	bus0: The internal bus# of IIO and also PCH. Configuration requests that target Devices 16-31 on this bus number must be forwarded to the PCH by the IIO. Devices 0-15 on this bus number are claimed to send to IIO internal registers.

6.6.34 lmmiol_base

Local MMIO Low Base.

Type: CFG Bus: 0 Offset: 0x10c		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:8	RW_LB	0x0	base: Corresponds to A[31:24] of MMIOL base address. An inbound memory address that satisfies 'local MMIOL base[15:8] <= A[31:24] <= local MMIOL limit[15:8]' is treated as a local peer-to-peer transaction that do not cross coherent interface. Note: Setting LMMIOL.BASE greater than LMMIOL.LIMIT disables local MMIOL peer-to-peer. This register is programmed once at boot time and does not change after that, including any quiesce flows.

6.6.35 lmmiol_limit

Local MMIO Low Limit.

Type: CFG Bus: 0 Offset: 0x10e		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:8	RW_LB	0x0	limit: Corresponds to A[31:24] of MMIOL limit. An inbound memory address that satisfies 'local MMIOL base[15:8] <= A[31:24] <= local MMIOL limit[15:8]' is treated as a local peer-to-peer transaction that does not cross the coherent interface. Note: Setting LMMIOL.BASE greater than LMMIOL.LIMIT disables local MMIOL peer-to-peer. This register is programmed once at boot time and does not change after that, including any quiesce flows.

6.6.36 lmmioh_base

Local MMIO High Base.

Type: CFG Bus: 0 Offset: 0x110		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
50:26	RW_LB	0x0	base: Corresponds to A[50:26] of MMIOH base. An inbound memory address that satisfies local MMIOH base [50:26] <= A[63:26] <= local MMIOH limit [50:26] is treated as a local peer-to-peer transaction that does not cross the coherent interface. Notes: Setting LMMIOH.BASE greater than LMMIOH.LIMIT disables local MMIOH peer-to-peer. This register is programmed once at boot time and does not change after that, including any quiesce flows.

6.6.37 lmmioh_limit

Local MMIO High Limit.

Type: CFG Bus: 0 Offset: 0x118		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
50:26	RW_LB	0x0	Local LMMIOH Limit:Address Corresponds to A[50:26] of Local MMIOH Limit (and Base) Address. An inbound memory address that satisfies the Local MMIO Base Address [50:26] <=A[63:26] <=Local MMIOH Limit Address [50:26], with A[63:51] equal to zero, is treated as a local peer2peer transaction that does not cross the coherent interface (ring). Notes: Setting LMMIOH.BASE greater than LMMIOH.LIMIT disables local MMIOH peer-to-peer. This register is programmed once at boot time and does not change after that, including any quiesce flows.

6.6.38 cipctrl

Coherent Interface Protocol Control.

Type: CFG Bus: 0 Offset: 0x140		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW	0x0	flushpendwr: Whenever this bit is written to 1 (regardless what the current value of this bit is), IRP block first clears bit 0 in CIPSTS register and takes a snapshot of the currently pending write transactions to dram in Write Cache, wait for them to complete fully (i.e. deallocate the corresponding Write CacheRRB entry) and then set bit 0 in CIPSTS register.
30:30	RW	0x0	adr_snapshot_req: Whenever this bit is written to 1, this implies wr$ snapshot request was due to ADR. This is a status indication and does not cause the snapshot to occur.
28:28	RW	0x0	diswrupdtflow: When set, PCIWriteUpdate command is never issued on IDI and the writes that triggered this flow would be treated as 'normal' writes and the rules corresponding to the 'normal writes' apply.
15:15	RW	0x1	rd_merge_enable:
12:12	RW-LB	0x0	dcaen: When clear, PrefetchHint will not be sent on the coherent interface. The CIPDCASAD table is programmed by BIOS and this bit is set when the table is valid.
10:10	RW-LB	0x1	vcp_pri_en: Give VCp transactions high priority in IRP and set pri=3 when issuing VCp transactions to the ring.
9:9	RW-LB	0x1	vc1_pri_en: Give VC1/m transactions high priority in IRP and set pri=3 when issuing VC1/m transactions to the ring.
8:8	RW	0x0	diswrcomb: Disables wr->wr, rd->rd, and rd->wr transfers. This bit is a don't-care if rd_merge_enable==1. Setting diswrcomb==1 and rd_merge_enable==0 disables all entry to entry transfers in IRP (causing a Cbo request for every switch request).
7:4	RW-LB	0x0	numrtids_isoc_pool1: Limits the number of RTIDs used for VC1/VCp/VCm isoch by Home Agent pool 1. BIOS programs value into this register based on SKU. An encoding of 0 in either numrtids_isoc_pool0 or numrtids_isoc_pool1 disables IIO isoch RTID allocation (useful for VCm in non-isoch systems or for debug). 12-15 are illegal values for this register.
3:0	RW-LB	0x0	numrtids_isoc_pool0: Limits the number of RTIDs used for VC1/VCp/VCm isoch by HA pool 0. BIOS programs value into this register based on SKU. An encoding of 0 in either numrtids_isoc_pool0 or numrtids_isoc_pool1 disables IIO isoch RTID allocation (useful for VCm in non-isoch systems or for debug). 12-15 are illegal values for this register.

6.6.39 cipsts

Coherent Interface Protocol Status.

Type: CFG Bus: 0 Offset: 0x144		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
2:2	RO_V	0x1	rrb_non_phold_arb_empty: This indicates that there are no pending requests in the RRB with the exception of ProcLock / Unlock messages to the lock arbiter. 0 - Pending RRB requests 1 - RRB Empty except for any pending Proclock / Unlock This is a live bit and hence can toggle clock by clock. This is provided mostly as a debug visibility feature.
1:1	RO_V	0x1	rrb_empty: This indicates that there are no pending requests in the RRB. 0 - Pending RRB requests 1 - RRB Empty This is a live bit and hence can toggle clock by clock. This is provided mostly as a debug visibility feature.
0:0	RO_V	0x0	flush_pending_writes: This bit gets cleared whenever bit 31 in CPICTRL is written to 1 by software and gets set by hw when the pending writes in the Write Cache (at the time bit 31 in CIPCTRL is written to 1 by software) complete i.e. the Write Cache/ RRB entry is deallocated for all those writes.

6.6.40 cipdcasad

Coherent Interface Protocol DCA Source Address Decode.

Type: CFG Bus: 0 Offset: 0x148		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:28	RW	0x0	dcalt7: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 7 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.
27:24	RW	0x0	dcalt6: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 6 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.
23:20	RW	0x0	dcalt5: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 5 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.
19:16	RW	0x0	dcalt4: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 4 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.
15:12	RW	0x0	dcalt3: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 3 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.

Type: CFG Bus: 0 Offset: 0x148	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
11:8	RW	0x0	dcalt2: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 2 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.
7:4	RW	0x0	dcalt1: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 1 NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.
3:0	RW	0x0	dcalt0: For a TPH/DCA request, specifies the target NodeID[3:0] when the inverted Tag[2:0] is 0. NID[2]==1 disables PrefetchHint issue for ST that maps to this entry.

6.6.41 cipintrc

Coherent Interface Protocol Interrupt Control.

Type: CFG Bus: 0 Offset: 0x14c	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
25:25	RW	0x0	dis_intx_route2ich:
24:24	RW	0x0	route_nmi2mca: Route NMI to MCA
18:18	RW	0x0	smi_msi_en: Intel SMI MSI Enable
17:17	RW	0x0	init_msi_en: INIT MSI Enable
16:16	RW	0x0	nmi_msi_en: NMI MSI Enable
11:11	RW	0x1	intr_mask: INTR Mask
10:10	RW	0x1	smi_mask: Intel SMI Mask
9:9	RW	0x1	init_mask: INIT Mask
8:8	RW	0x1	nmi_mask: NMI Mask
1:1	RW	0x0	logical:

6.6.42 cipintrs

Coherent Interface Protocol Interrupt Status.

This register is to be polled by BIOS to determine if internal pending system interrupts are drained out of IIO. General usage model is for software to quiesce the source e.g. IOM global error logic of a system event like Intel SMI, then poll this register till this register indicates that the event is not pending inside IIO. One additional read is required from software, after the register first reads 0 for the associated event.

Type: CFG Bus: 0 Offset: 0x154		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW1CS	0x0	Intel SMI: This is set whenever IIO forwards a VLW from PCH that had the Intel SMI bit asserted
30:30	RW1CS	0x0	nmi: This is set whenever IIO forwards a VLW from PCH that had the NMI bit asserted
7:7	RO_V	0x0	mca_ras_evt_pending: MCA RAS Event Pending
6:6	RO_V	0x0	nmi_ras_evt_pending: NMI RAS Event Pending
5:5	RO_V	0x0	smi_ras_evt_pending: Intel SMI RAS Event Pending
4:4	RO_V	0x0	intr_evt_pending: Intel SMI RAS Event Pending
2:2	RO_V	0x0	init_evt_pending: Intel SMI RAS Event Pending
1:1	RO_V	0x0	nmi_evt_pending: Intel SMI RAS Event Pending
0:0	RO_V	0x0	vlw_msgpend: VLW Message Pending, either generated internally or externally

6.6.43 vtbar

Base Address Register for Intel VT-d.

Type: CFG Bus: 0 Offset: 0x180		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:13	RW_LB	0x0	vtd_chipset_base_address: Provides an aligned 8K base address for IIO registers relating to Intel VT-d. All inbound accesses to this region are completer aborted by the IIO.
0:0	RW_LB	0x0	vtd_chipset_base_address_enable: Note that accesses to registers pointed to by VTBAR are accessible via message channel, irrespective of the setting of this enable bit i.e. even if this bit is clear, read/write to Intel VT-d registers are completed normally (writes update registers and reads return the value of the register) for accesses from message channel. This bit is RW-LB i.e. lock is determined based on the 'trusted' bit in message channel when VTGENCTRL[15] is set, else it is RO.

6.6.44 vtgenctrl

Intel VT-d General Control.

Type: CFG Bus: 0 Offset: 0x184		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:15	RW_O	0x0	lockvtd: When this bit is 0, the VTBAR[0] is RW-LB, else it is RO.
7:4	RW_LB	0xa	hpa_limit: Represents the host processor addressing limit 0000: 2^36 (i.e. bits 35:0) 0001: 2^37 (i.e. bits 36:0) ... 1010: 2^46 (i.e. bits 45:0) When Intel VT-d translation is enabled on an Intel VT-d engine, all host addresses (during page walks) that go beyond the limit specified in this register will be aborted by IIO. Note that pass-through and 'translated' ATS accesses carry the host-address directly in the access and are subject to this check as well.
3:0	RW_LB	0x8	gpa_limit: Represents the guest virtual addressing limit for the non-Isoch Intel VT-d engine. 0000: 2^40 (i.e. bits 39:0) 0001: 2^41 (i.e. bits 40:0) .. 0111: 2^47 1000: 2^48 Others: Reserved When Intel VT-d translation is enabled, all incoming guest addresses from PCI Express, associated with the non-isoch Intel VT-d engine, that go beyond the limit specified in this register will be aborted by IIO and a UR response returned. This register is not used when translation is not enabled. Note that 'translated' and 'pass-through' addresses are in the 'host-addressing' domain and NOT 'guest-addressing' domain and hence GPA_LIMIT checking on those accesses are bypassed and instead HPA_LIMIT checking applies.

6.6.45 vtgenctrl2

Intel VT-d General Control 2.

Type: CFG Bus: 0 Offset: 0x18c		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
18:12	RW_LB	0x4	tlb_free_entry_limit: Retry prefetch request when number of entries available for allocation in the IOTLB is less than the programmed value. Set this to 0 to disable it.

Type: CFG Bus: 0 Offset: 0x18c		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
11:11	RW_LB	0x0	lructrl: Controls what increments the LRU counter that is used to degrade the LRU bits in the IOTLB, L1/L2, and L3 caches. 1: Count Cycles same as TB 0: Count Requests
10:7	RW_LB	0x7	lt: Controls the rate at which the LRU buckets should degrade. If we are in “Request” mode (LRUCTRL = 0), then we will degrade LRU after 16 * N requests where N is the value of this field. If we are in “Cycles” mode (LRUCTRL = 1), then we will degrade LRU after 256 * N cycles where N is the value of this field.
3:3	RW_LB	0x0	ignoreubitleafeviction: Do not use U bit in leaf entry for leaf eviction policy on untranslated DMA requests (AT=00b)
2:2	RW_LB	0x0	evictnonleafat01: Mark non-leaf entries on translation requests with AT=01 for early eviction
1:1	RW_LB	0x0	dontevictleafat01: Do not mark leaf entries with U=0 on translation requests with AT=01 for early eviction

6.6.46 iotlbpartition

IOTLB Partitioning Control.

Type: CFG Bus: 0 Offset: 0x194		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
28:27	RW	0x0	rangesel_dmi_20_22: Range Selection for DMI[20:22]
26:25	RW	0x0	rangesel_iou24_upper_x2: Range Selection for IOU24 upper X2 link
24:23	RW	0x0	rangesel_iou23_upper_x2: Range Selection for IOU23 upper X2 link
14:13	RW	0x0	rangesel_me: Range Selection for ME
12:11	RW	0x0	rangesel_cb: Range Selection for Intel QuickData Technology.
10:9	RW	0x0	rangesel_intr: Range Selection for INTR
0:0	RW_LB	0x0	iotlb_parten: 0: Disabled 1: Enabled

6.6.47 vtuncerrsts

Intel VT-d Uncorrectable Error Status.

Type: CFG Bus: 0 Offset: 0x1a8		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW1CS	0x0	vtderr: When set, this bit is set when an Intel VT-d spec defined error has been detected (and logged in the Intel VT-d fault registers)
8:8	RW1CS	0x0	protmemviol: Protected memory region space violated status
7:7	RW1CS	0x0	miscerrs: This error bit is set when TE is off DMA/INTR request has AT set to nonzero value.
6:6	RW1CS	0x0	unsucc_ci_rdcp: Unsuccessful status received in the coherent interface read completion status.
5:5	RW1CS	0x0	perr_tlb1: TLB1 Parity Error Status.
4:4	RW1CS	0x0	perr_tlb0: TLB0 Parity Error Status.
3:3	RW1CS	0x0	perr_l3_lookup: Data Parity error while doing a L3 lookup status.
2:2	RW1CS	0x0	perr_l1_lookup: Data Parity error while doing a L1 lookup status. Note the mapping of this register field varies over the mapping in tuncerrmsk and vtuncerrsev.
1:1	RW1CS	0x0	perr_l2_lookup: Data Parity error while doing a L1 lookup status. Note the mapping of this register field varies over the mapping in tuncerrmsk and vtuncerrsev.
0:0	RW1CS	0x0	perr_context_cache:

6.6.48 vtuncerrmsk

Intel VT-d Uncorrectable Error Mask.

Mask out error reporting to IIO. Bit 31 should always be set to 1. It is recommend that the other bits be left as zero so these internal errors are reported out.

Setting bits will not prevent any error collecting inside of Intel VT-d in the Intel VT-d Fault Recording Registers.

Type: CFG Bus: 0 Offset: 0x1ac		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RWS	0x1	vtderr_msk: This bit should be set to 1 by BIOS. It is highly recommended that this bit is never set to 0. If Intel VT-d errors are configured to be fatal, leaving this bit set to 0 will cause Fatal errors to be reported when devices send illegal requests. This is generally undesireable.
8:8	RWS	0x0	protmemviol_msk: Protected memory region space violated mask
7:7	RWS	0x0	miscerrm: miscerrm mask Illegal request to 0xFEE, GPAHPA limit error mask
6:6	RWS	0x0	unsucc_ci_rdcp_msk: Unsuccessful status received in the coherent interface read completion mask.
5:5	RWS	0x0	perr_tlb1_msk: TLB1 Parity Error mask
4:4	RWS	0x0	perr_tlb0_msk: TLB0 Parity Error mask
3:3	RWS	0x0	perr_l3_lookup_msk: Data Parity error while doing a L3 lookup mask
2:2	RWS	0x0	perr_l2_lookup_msk: Data Parity error while doing a L2 lookup mask
1:1	RWS	0x0	perr_l1_lookup_msk: Data Parity error while doing a L1 lookup mask
0:0	RWS	0x0	perr_context_cache_msk: Data Parity error while doing a context cache lookup mask.

6.6.49 vtuncerrsev

Intel VT-d Uncorrectable Error Severity.

Type: CFG Bus: 0 Offset: 0x1b0		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RWS	0x0	vtderr_sev: When set, this bit escalates reporting of Intel VT-d spec defined errors, as FATAL errors. When clear, those errors are escalated as Nonfatal errors. Setting this bit to a 1 can allow a guest VM to trigger an unrecoverable FATAL error at the platform. It is HIGHLY recommended that BIOS keep this bit set to 0, as such behavior is generally undesirable.
8:8	RWS	0x1	protmemviol_sev: Protected memory region space violated severity.
7:7	RWS	0x1	miscerrsev: miscerrsev severity. Illegal request to 0xFEE, GPAHPA limit error severity
6:6	RWS	0x0	unsucc_ci_rdcp_sev: Unsuccessful status received in the coherent interface read completion severity.
5:5	RWS	0x1	perr_tlb1_sev: TLB1 Parity Error severity.
4:4	RWS	0x1	perr_tlb0_sev: TLB1 Parity Error severity.
3:3	RWS	0x1	perr_l3_lookup_sev: Data Parity error while doing a L3 lookup severity.
2:2	RWS	0x1	perr_l2_lookup_sev: Data Parity error while doing a L2 lookup severity.
1:1	RWS	0x1	perr_l1_lookup_sev: Data Parity error while doing a L1 lookup severity.
0:0	RWS	0x1	perr_context_cache_sev: Data Parity error while doing a context cache lookup severity.

6.6.50 vtuncerrptr

Intel VT-d Uncorrectable Error Pointer.

Type: CFG Bus: 0 Offset: 0x1b4		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
4:0	ROS_V	0x0	vt_uncferr_ptr: This field points to which of the unmasked uncorrectable errors happened first. This field is only valid when the corresponding error is unmasked and the status bit is set and this field is rearmed to load again when the status bit indicated to by this pointer is cleared by software from 1 to 0. Value of 0x0 corresponds to bit 0 in VTUNCERRSTS register, value of 0x1 corresponds to bit 1 and so forth.

6.6.51 iiomiscctrl

IIO MISC Control.

Type: CFG Bus: 0 Offset: 0x1c0			PortID: N/A Device: 5 Function: 0
Bit	**Attr**	**Default**	**Description**
41:41	RW	0x0	en_poismsg_spec_behavior: A received poison packet is treated as a Fatal error if it's severity bit is set, but treated as a correctable if the severity bit is cleared and logged in both the UNCERRSTS register and the Advisory Non-Fatal Error bit in the CORERRSTS register. When this bit is clear: sev pfen error 0 0 non-fatal 0 1 correctable 1 0 fatal 1 1 correctable When this bit is set: sev pfen error 0 0 non-fatal 0 1 correctable 1 0 fatal 1 1 fatal
40:40	RW	0x0	enable_io_mca:
37:37	RW	0x0	poisfen: Enables poisoned data received inbound (either inbound posted data or completions for outbound reads that have poisoned data) to be forwarded to the destination (DRAM or Cache or PCIe Peer). 0: Poison indication is not forwarded with the data (this may result in silent corruption if AER poison reporting is disabled.) 1: Poison indication is forwarded with the data (this may result in a conflict with MCA poison reporting if AER poison reporting is enabled)
33:33	RWS	0x0	force_6b_mc_group: 0 = Use 4 bits for Dualcast group 1 = Use 6 bits for Dualcast group
25:25	RWS	0x1	cballocen: When set, use Allocating Flows for non-DCA writes from Intel QuickData Technology DMA. This bit does not affect DCA requests when DCA requests are enabled (bit 21 of this register). A DCA request is identified as matching the DCA requestor ID and having a Tag of non-zero. All DCA requests are always allocating, unless they are disabled, or unless all allocating flows are disabled (bit 24). If all allocating flows are disabled, then DCA requests are also disabled. BIOS is to leave this bit at default of 1b for all but DMI port.
24:24	RW	0x0	disable_all_allocating_flows: When this bit is set, IIO will no more issue any new inbound IDI command that can allocate into LLC. Instead, all the writes will use one of the non-allocating commands - PCIWiL/PCIWiLF/PCINSWr/PCINSWrF. Software should set this bit only when no requests are being actively issued on IDI. So either a lock/quiesce flow should be employed before this bit is set/cleared or it should be set up before DMA is enabled in system.

Type: CFG Bus: 0 Offset: 0x1c0		PortID: N/A Device: 5	Function: 0

Bit	Attr	Default	Description
19:19	RW	0x0	rvgaen: Remote VGA Enable Enables VGA accesses to be sent to remote node. If set, accesses to the VGA region (A_0000 to B_FFFF) will be forwarded to the CBo where it will determine the NodeID where the VGA region resides. It will then be forwarded to the given remote node. If clear, then VGA accesses will be forwarded to the local PCIe port that has it's VGAEN set. If none have their VGAEN set, then the request will be forwarded to the local DMI port, if operating in DMI mode. If it is not operating in DMI mode, then the request will be aborted.
18:18	RW	0x1	disable_inbound_ro_for_vc0: When enabled this mode will treat all inbound write traffic as RO = 0 for VC0. This affects all PCI Express ports and the DMI port.0 - Ordering of inbound transactions is based on RO bit for VC0 1 - RO bit is treated as '0' for all inbound VC0 traffic Note that this pretty much impacts only the NS write traffic because for snooped traffic RO bit is ignored by h/w. When this bit is set, the NS write if enabled BW is going to be generally bad. Note that this bit does not impact VC1 and VCm writes
17:16	RW	0x1	dmi_vc1_write_ordering: Mode is used to control VC1 write traffic from DMI (Intel VT). 00: Reserved 01: Serialize writes on CSI issuing one at a time 10: Pipeline writes on CSI except for writes with Tag value of 0x21 which are issued only after prior writes have all completed and reached global observability 11: Pipeline writes on CSI based on RO bit i.e. if RO = 1, pipeline a write on Intel QPI without waiting for prior write to have reached global observability. If RO0, then it needs to wait till prior writes have all reached global observability.
15:15	RW	0x0	dmi_vc1_vt_d_fetch_ordering: This mode is to allow VC1 Intel VT-d conflicts with outstanding VC0 Intel VT-d reads on IDI to be pipelined. This can occur when Intel VT-d tables are shared between Intel VT (VC1) and other devices. To ensure QoS the Intel VT-d reads from VC1 need to be issued in parallel with non-Isoc accesses to the same cacheline. 0: Serialize all IDI address conflicts to DRAM 1: Pipeline Intel VT-d reads from VC1 with address conflict on IDI Notes: A maximum of 1 VC1 Intel VT-d read and 1 non-VC1 Intel VT-d read to the same address can be outstanding on IDI.
13:13	RW	0x0	vc1_reads_bypass_writes: 0: VC1 Reads push VC1 writes 1: VC1 Reads are allowed to bypass VC1 writes
12:12	RW	0x0	lock_thaw_mode: Mode controls how inbound queues in the south agents (PCIe, DMI) thaw when they are target of a locked read. 0: Thaw only posted requests 1: Thaw posted and non-posted requests. Note that if the lock target is also a 'problematic' port (as indicated by bit 38 in MISCCTRLSTS register), then this becomes meaningless because both posted and non-posted requests are thawed.

Type: CFG Bus: 0 Offset: 0x1c0		PortID: N/A Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
10:10	RW	0x0	legacy_port: Sockets where the NodeID = 0 are generally identified as having the legacy DMI port. But there is still a possibility that another socket also has a NodeID = 0. The system is configured by software to route legacy transactions to the correct socket. However, inbound legacy messages received on a PCIe port of a socket with NodeID = 0 that is not the true legacy port need to be routed to a remote socket that is the true legacy port. For a local NodeID is zero, this bit is used to determine if inbound messages should be routed to a DMI port on a remote socket with NodeID = 0, or if the messages should be sent to the local DMI port, since the local NodeID is also 0. If the local NodeID is not zero, then this bit is ignored. 0: indicates this socket has the true DMI legacy port, send legacy transactions to local DMI port 1: indicates this is a non-legacy socket, send legacy transactions to the Coherent Interface Notes: This bit does not affect routing for non-message transactions. It only affects inbound messages that need to be routed to the true legacy port. This bit is NOT used for any outbound address decode routing purposes. Outbound traffic that is subtractively decoded will always be forwarded to local DMI port, if one exists, or it will be aborted. The default value of this field is based on the NodeID and FWAGENT_DMIMODE straps. Software can only change this bit after reset during early boot phase, but must guarantee there is no traffic flowing through the system, except for the write that changes this bit.
8:8	RW	0x0	tocmvalid: Enables the TOCM field.
7:3	RW	0xe	tocm: Indicates the top of Core physical addressability limit. 00000-00100: Reserved 00101: 2^37 00110: 2^38 ... 1110: 2^46 01111 -11111: Reserved IIO uses this to abort all inbound transactions that cross this limit.
2:2	RW	0x0	en1k: This bit when set, enables 1K granularity for IO space decode in each of the virtual P2P bridges corresponding to root ports, and DMI ports.
1:1	RWS_O	0x0	uniphy_disable: Place entire UNIPHY in L2 for when no ports are used, as in some multi-socket configurations

6.6.52 ltdpr

Intel TXT DMA Protected Range.

General Description: This register holds the address and size of the DMA protected memory region for Intel® Trusted Execution Technology (Intel® TXT) MP usage.

Type: CFG Bus: 0 Offset: 0x290	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
31:20	RO_V	0x0	topofdpr: Top address + 1 of DPR. This is RO, and it is copied by HW from TSEGBASE[31:20].
11:4	RW_L	0x0	size: This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255 MB. The amount of memory reported in this field will be protected from all DMA accesses. The top of the protected range is typically the BASE of TSEG -1. BIOS is expected to program that in to bits 31:20 of this register. Notes: If TSEG is not enabled, then the top of this range becomes the base ME stolen space, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range - Generic Protected ranges, TSEG range, Intel VT-d tables, Intel VT-d protection ranges, MMCFG protection range and is done post any Intel VT-d translation or Intel TXT checks. Therefore incoming cycles are checked against this range after the Intel VT-d translation and faulted if they hit this protected range, even if they passed the Intel VT-d translation. All the memory checks are OR'ed with respect to NOT being allowed to go to memory. So if either Generic protection range, DPR, Intel VT-d, TSEG range disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all the above checks must pass before a cycle is allowed to DRAM. DMA remap engines are allowed to access the DPR region without any faulting. It is always legal for any DMA remap engine to read or write into the DPR region, thus DMA remap accesses must not be checked against the DPR range.
2:2	RW_L	0x0	commandbit: Writing a '1' to this bit will enable protection. Writing a '0' to this bit will disable protection.
1:1	RO	0x0	protregsts: IIO sets this bit when the protection has been enabled in hardware and for all practical purposes this should be immediate. When protection is disabled, then this bit is clear
0:0	RW_O	0x0	lock: Bits 19:0 are locked down in this register when this bit is set. Can this be set while other bits are being written to in the same write transaction

6.6.53 lcfgbus_base

Type: CFG Bus: 0 Offset: 0x41c	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	lcfgbus_base:

6.6.54 lcfgbus_limit

Type: CFG Bus: 0 Offset: 0x41d	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	lcfgbus_limit:

6.6.55 csipintrs

Type: CFG Bus: 0 Offset: 0x450	PortID: N/A Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
7:7	RO_V	0x0	mca_ras_evt_pend: MCA event interrupt pended.
6:6	RO_V	0x0	nmi_ras_evt_pend: NMI RAS event interrupt pended.
5:5	RO_V	0x0	smi_ras_evt_pend: Intel SMI RAS event interrupt pended.
4:4	RO_V	0x0	intr_evt_pend: Intr event interrupt pended.
2:2	RO_V	0x0	init_evt_pend: Init event interrupt pended.
1:1	RO_V	0x0	nmi_evt_pend: NMI event interrupt pended.
0:0	RO_V	0x0	smi_evt_pend: Intel SMI event interrupt pended.

6.7 Device 5 Function 0 MMIO Region VTBAR

Intel VT-d registers are all addressed using aligned dword or aligned qword accesses. Any combination of bits is allowed within a dword or qword access. The Intel VT-d remap engine registers corresponding to the port represented by Device 0, occupy the first 4 K of offset starting from the base address defined by VTBAR register.

Register Name	Offset	Size
vtd0_version	0x0	32
vtd0_cap	0x8	64
vtd0_ext_cap	0x10	64
vtd0_glbcmd	0x18	32
vtd0_glbsts	0x1c	32
vtd0_rootentryadd	0x20	64
vtd0_ctxcmd	0x28	64
vtd0_fltsts	0x34	32
nonisoch_fltevtctrl	0x38	32

Register Name	Offset	Size
nonisoch_fltevtdata	0x3c	32
vtd0_fltevtaddr	0x40	32
vtd0_fltevtupraddr	0x44	32
vtd0_pmen	0x64	32
vtd0_prot_low_mem_base	0x68	32
vtd0_prot_low_mem_limit	0x6c	32
vtd0_prot_high_mem_base	0x70	64
vtd0_prot_high_mem_limit	0x78	64
vtd0_inv_queue_head	0x80	64
vtd0_inv_queue_tail	0x88	64
vtd0_inv_queue_add	0x90	64
vtd0_inv_comp_status	0x9c	32
nonisoch_inv_cmp_evtctrl	0xa0	32
nonisoch_invevtdata	0xa4	32
vtd0_inv_comp_evt_addr	0xa8	32
vtd0_inv_comp_evt_upraddr	0xac	32
vtd0_intr_remap_table_base	0xb8	64
vtd0_fltrec0_gpa	0x100	64
vtd0_fltrec0_src	0x108	64
vtd0_fltrec1_gpa	0x110	64
vtd0_fltrec1_src	0x118	64
vtd0_fltrec2_gpa	0x120	64
vtd0_fltrec2_src	0x128	64
vtd0_fltrec3_gpa	0x130	64
vtd0_fltrec3_src	0x138	64
vtd0_fltrec4_gpa	0x140	64
vtd0_fltrec4_src	0x148	64
vtd0_fltrec5_gpa	0x150	64
vtd0_fltrec5_src	0x158	64
vtd0_fltrec6_gpa	0x160	64
vtd0_fltrec6_src	0x168	64
vtd0_fltrec7_gpa	0x170	64
vtd0_fltrec7_src	0x178	64
vtd0_invaddrreg	0x200	64
vtd0_iotlbinv	0x208	64
vtd1_version	0x1000	32
vtd1_cap	0x1008	64
vtd1_ext_cap	0x1010	64
vtd1_glbcmd	0x1018	32
vtd1_glbsts	0x101c	32
vtd1_rootentryadd	0x1020	64
vtd1_ctxcmd	0x1028	64
vtd1_fltsts	0x1034	32

Register Name	Offset	Size
vtd1_fltevtaddr	0x1040	32
vtd1_fltevtupraddr	0x1044	32
vtd1_pmen	0x1064	32
vtd1_prot_low_mem_base	0x1068	32
vtd1_prot_low_mem_limit	0x106c	32
vtd1_prot_high_mem_base	0x1070	64
vtd1_prot_high_mem_limit	0x1078	64
vtd1_inv_queue_head	0x1080	64
vtd1_inv_queue_tail	0x1088	64
vtd1_inv_queue_add	0x1090	64
vtd1_inv_comp_status	0x109c	32
vtd1_inv_comp_evt_addr	0x10a8	32
vtd1_inv_comp_evt_upraddr	0x10ac	32
vtd1_intr_remap_table_base	0x10b8	64
vtd1_fltrec0_gpa	0x1100	64
vtd1_fltrec0_src	0x1108	64
vtd1_invaddrreg	0x1200	64
vtd1_iotlbinv	0x1208	64

6.7.1 vtd[0:1]_version

Intel VT-d Version Number.

Type: MEM Bus: 0 Offset: 0x0, 0x1000		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:4	RO	0x1	major_revision:
3:0	RO	0x0	minor_revision:

6.7.2 vtd[0:1]_cap

Intel VT-d Capabilities.

Type: MEM Bus: 0 Offset: 0x8, 0x1008		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
59:59	RW_O	0x1	posted_interrupts_support: The processor supports posted interrupts
55:55	RO	0x1	dma_read_draining: The processor supports hardware based draining
54:54	RO	0x1	dma_write_draining: The processor supports hardware based write draining

Type: MEM Bus: 0 Offset: 0x8, 0x1008		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
53:48	RO	0x12	mamv: The processor support MAMV value of 12h (up to 1G super pages).
47:40	RO	0x7	number_of_fault_recording_registers: The processor supports 8 fault recording registers
39:39	RO	0x1	page_selective_invalidation: Supported in IIO
37:34	RW_O	0x3	super_page_support: 2 MB, 1G supported.
33:24	RO	0x10	fault_recording_register_offset: Fault registers are at offset 100h
23:23	RO	0x0	spatial_separation:
22:22	RO	0x1	zlr: Zero-length DMA requests to write-only pages supported.
21:16	RO_V	0x2f	mgaw: This register is set by the processor-based on the setting of the GPA_LIMIT register. The value is the same for both the Intel VT and non-Intel VT engines. This is because the translation for Intel VT has been extended to be 4-level (instead of 3).
12:8	RO	0x4	sagaw: Supports 4-level walk on both Intel VT and non-Intel VT engines
7:7	RO	0x0	tcm: The processor does not cache invalid pages. This bit should always be set to 0 on HW. It can be set to one when we are doing software virtualization of Intel VT-d.
6:6	RO	0x1	phmr_support: The processor supports protected high memory range
5:5	RO	0x1	plmr_support: The processor supports protected low memory range
4:4	RO	0x0	rwbf:
3:3	RO	0x0	advanced_fault_logging: The processor does not support advanced fault logging
2:0	RO	0x6	number_of_domains_supported: The processor supports 256 domains with 8 bit domain ID

6.7.3 vtd[0:1]_ext_cap

Extended Intel VT-d Capability.

Type: MEM Bus: 0 Offset: 0x10, 0x1010		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
23:20	RO	0xf	maximum_handle_mask_value: IIO supports all 16 bits of handle being masked. Note IIO always performs global interrupt entry invalidation on any interrupt cache invalidation command and h/w never really looks at the mask value.
17:8	RO	0x20	invalidation_unit_offset: IIO has the invalidation registers at offset 200h

Type: MEM Bus: 0 Offset: 0x10, 0x1010		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
7:7	RO	0x1	snoop_control: 0: Hardware does not support 1-setting of the SNP field in the page-table entries. 1: Hardware supports the 1-setting of the SNP field in the page-table entries. IIO supports snoop override only for the non-isoch Intel VT-d engine
6:6	RO	0x1	pass_through: IIO supports pass through.
4:4	RW_O	0x1	ia32_extended_interrupt_mode: IIO supports the extended interrupt mode
3:3	RO	0x1	interrupt_remapping_support: IIO supports this
2:2	RW_O	0x1	device_tlb_support: IIO supports ATS for the non-isoch Intel VT-d engine. This bit is RW-O for non-isoch engine. For VTD[0]_EXT_CAP.Bit[2] the default is 1, but can be programmed to 0. Clarification: For VTD[1]_EXT_CAP.Bit[2] the default is 0
1:1	RO	0x1	queued_invalidation_support: IIO supports this. For VTD[1]_EXT_CAP.Bit[1] the default is 0.
0:0	RW_O	0x0	coherency_support: BIOS can write to this bit to indicate to hardware to either snoop or not-snoop the DMA/Interrupt table structures in memory (root/context/pd/pt/irt). Note that this bit is expected to be always set to 0 for the Intel VT-d engine and programmability is only provided for that engine for debug reasons.

6.7.4 vtd[0:1]_glbcmd

Intel VT-d Global Command.

Type: MEM Bus: 0 Offset: 0x18, 0x1018		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW	0x0	translation_enable: Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware 1: Enable DMA-remapping hardware Hardware reports the status of the translation enable operation through the TES field in the Global Status register. Before enabling (or re-enabling) DMA-remapping hardware through this field, software must: - Setup the DMA-remapping structures in memory - Flush the write buffers (through WBF field), if write buffer flushing is reported as required. - Set the root-entry table pointer in hardware (through SRTP field). - Perform global invalidation of the context-cache and global invalidation of IOTLB - If advanced fault logging supported, setup fault log pointer (through SFL field) and enable advanced fault logging (through EAFL field). There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all.

Type: MEM Bus: 0 Offset: 0x18, 0x1018		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
30:30	RW_V	0x0	set_root_table_pointer: Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register.Hardware reports the status of the root table pointer set operation through the RTPS field in the Global Status register. The root table pointer set operation must be performed before enabling or re-enabling (after disabling) DMA remapping hardware. After a root table pointer set operation, software must globally invalidate the context cache followed by global invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not any stale cached entries. While DMA-remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root table pointer. Clearing this bit has no effect.
29:29	RO	0x0	set_fault_log_pointer:
28:28	RO	0x0	enable_advanced_fault_logging:
27:27	RO	0x0	write_buffer_flush:
26:26	RW	0x0	queued_invalidation_enable: Software writes to this field to enable queued invalidations. 0: Disable queued invalidations. In this case, invalidations must be performed through the Context Command and IOTLB Invalidation Unit registers. 1: Enable use of queued invalidations. Once enabled, all invalidations must be submitted through the invalidation queue and the invalidation registers cannot be used till the translation has been disabled. The invalidation queue address register must be initialized before enabling queued invalidations. Also software must make sure that all invalidations submitted prior via the register interface are all completed before enabling the queued invalidation interface.
25:25	RW	0x0	interrupt_remapping_enable: 0: Disable Interrupt Remapping Hardware 1: Enable Interrupt Remapping Hardware Hardware reports the status of the interrupt-remap enable operation through the interrupt_remapping_enable field in the Global Status register. Before enabling (or re-enabling) Interrupt-remapping hardware through this field, software must: • Setup the interrupt-remapping structures in memory • Set the Interrupt Remap table pointer in hardware (through IRTP field). • Perform global invalidation of IOTLB There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. IIO must drain any in-flight translated DMA read/write, MSI interrupt requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the interrupt_remapping_enable field in the VTD[1:0_]GLBSTS. Value returned on read of this field is undefined.

Type: MEM Bus: 0 Offset: 0x18, 0x1018		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
24:24	RW_V	0x0	set_interrupt_remap_table_pointer: Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register. Hardware reports the status of the interrupt remapping table pointer set operation through the interrupt_remapping_table_pointer_status field in the Global Status register. The interrupt remap table pointer set operation must be performed before enabling or re-enabling (after disabling) interrupt remapping hardware through the interrupt_remapping_enable field. After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. IIO hardware internally clears this field before the 'set' operation requested by software has take effect.
23:23	RW	0x0	cfi: Compatibility Format Interrupt Software writes to this field to enable or disable Compatibility Format interrupts on Intel® 64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active. 0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the vtd[0:1]_glbsts register.

6.7.5 vtd[0:1]_glbsts

Intel VT-d Global Status.

Type: MEM Bus: 0 Offset: 0x1c, 0x101c		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RO_V	0x0	translation_enable_status: When set, indicates that translation hardware is enabled and when clear indicates the translation hardware is not enabled.
30:30	RO_V	0x0	set_root_table_pointer_status: This field indicates the status of the root- table pointer in hardware.This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware finishes the set root-table pointer operation (by performing an implicit global invalidation of the context-cache and IOTLB, and setting/updating the root-table pointer in hardware with the value provided in the Root-Entry Table Address register).
29:29	RO	0x0	set_fault_log_pointer_status:
28:28	RO	0x0	advanced_fault_logging_status:
27:27	RO	0x0	write_buffer_flush_status:

Type: MEM Bus: 0 Offset: 0x1c, 0x101c	PortID: 8'h7e Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
26:26	RO_V	0x0	queued_invalidation_interface_status: IIO sets this bit once it has completed the software command to enable the queued invalidation interface. Till then this bit is 0.
25:25	RO_V	0x0	interrupt_remapping_enable_status: OH sets this bit once it has completed the software command to enable the interrupt remapping interface. Till then this bit is 0.
24:24	RO_V	0x0	interrupt_remapping_table_pointer_status: This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23:23	RO_V	0x0	cfis: Compatibility Format Interrupt Status The value reported in this field is applicable only when interrupt-remapping is enabled and Legacy interrupt mode is active. 0: Compatibility format interrupts are blocked. 1: Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).

6.7.6 vtd[0:1]_rootentryadd

Intel VT-d Root Entry Table Address.

Type: MEM Bus: 0 Offset: 0x20, 0x1020	PortID: 8'h7e Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
63:12	RW	0x0	root_entry_table_base_address: 4K aligned base address for the root entry table. Software specifies the base address of the root-entry table through this register, and enables it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.

6.7.7 vtd[0:1]_ctxcmd

Intel VT-d Context Command.

Type: MEM Bus: 0 Offset: 0x28, 0x1028		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:63	RW_V	0x0	icc: Invalidate Context Entry Cache Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field to be clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must not submit another invalidation request through this register while the ICC field is set.Software must submit a context cache invalidation request through this field only when there are no invalidation requests pending at this DMA-remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed.
62:61	RW	0x0	cirg: Context Invalidation Request Granularity When requesting hardware to invalidate the context-entry cache (by setting the ICC field), software writes the requested invalidation granularity through this field.Following are the encoding for the 2-bit IRG field. 00: Reserved. Hardware ignores the invalidation request and reports invalidation complete by clearing the ICC field and reporting 00 in the CAIG field. 01: Global Invalidation request. 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. 11: Device-selective invalidation request. The target SID must be specified in the SID field, and the domain-id (programmed in the context-entry for this device) must be provided in the DID field. The processor aliases the h/w behavior for this command to the 'Domain-selective invalidation request'. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.
60:59	RO_V	0x0	caig: Context Actual Invalidation Granularity Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field). The following are the encoding for the 2-bit CAIG field. 00: Reserved. This is the value on reset. 01: Global Invalidation performed. The processor sets this in response to a global invalidation request. 10: Domain-selective invalidation performed using the domain-id that was specified by software in the DID field. The processor set this in response to a domain-selective or device-selective invalidation request. 11: Device-selective invalidation. The processor never sets this encoding.
33:32	RW	0x0	fm: Function Mask Used by the processor when performing device selective invalidation.
31:16	RW	0x0	source_id: Used by the processor when performing device selective context cache invalidation

Type: MEM Bus: 0 Offset: 0x28, 0x1028		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:0	RW	0x0	domain_id: Indicates the id of the domain whose context-entries needs to be selectively invalidated. S/W needs to program this for both domain and device selective invalidates. The processor ignores bits 15:8 since it supports only a 8 bit Domain ID.

6.7.8 vtd[0:1]_fltsts

Intel VT-d Fault Status.

Type: MEM Bus: 0 Offset: 0x34, 0x1034		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
15:8	ROS_V	0x0	fault_record_index: This field is valid only when the Primary Fault Pending field is set. This field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the Primary Fault pending field was set by hardware.
6:6	RW1CS	0x0	invalidation_timeout_error: Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register.
5:5	RW1CS	0x0	invalidation_completion_error: Hardware received an unexpected or invalid Device-IOTLB invalidation completion. At this time, a fault event is generated based on the programming of the Fault Event Control register.
4:4	RW1CS	0x0	invalidation_queue_error: Hardware detected an error associated with the invalidation queue. For example, hardware detected an erroneous or un-supported Invalidation Descriptor in the Invalidation Queue. At this time, a fault event is generated based on the programming of the Fault Event Control register.
1:1	ROS_V	0x0	primary_fault_pending: This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this DMA-remap hardware unit. 0: No pending faults in any of the fault recording registers 1: One or more fault recording registers has pending faults. The fault recording index field is updated by hardware whenever this field is set by hardware. Also, depending on the programming of fault event control register, a fault event is generated when hardware sets this field.
0:0	RW1CS	0x0	primary_fault_overflow: Hardware sets this bit to indicate overflow of fault recording registers

6.7.9 nonisoch_fltevtctrl

Fault Event Control.

Type: MEM Bus: 0 Offset: 0x38		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW	0x1	fault_nonisoch_msgmsk: 1: Hardware is prohibited from issuing interrupt message requests. 0: Software has cleared this bit to indicate interrupt service is available. When a faulting condition is detected, hardware may issue a interrupt request (using the fault event data and fault event address register values) depending on the state of the interrupt mask and interrupt pending bits.
30:30	RO_V	0x0	fault_nonisoch_msi_pend: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as when an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. - Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. - Hardware detected invalidation completion timeout error, setting the ICT field in the Fault Status register. - If any of the above status fields in the Fault Status register was already set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either (a) Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field. (b) Software servicing all the pending interrupt status fields in the Fault Status register. • PPF field is cleared by hardware when it detects all the Fault Recording registers have Fault (F) field clear. • Other status fields in the Fault Status register is cleared by software writing back the value read from the respective fields.
29:0	RO	0x0	fault_nonisoch_msgmsk_const:

6.7.10 nonisoch_fltevtdata

Fault Event Data.

Type: MEM Bus: 0 Offset: 0x3c		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RO	0x0	fault_nonisoch_data_const:
15:0	RW	0x0	fault_nonisoch_data:

6.7.11 vtd[0:1]_fltevtaddr

Intel VT-d Fault Event Address.

Type: MEM Bus: 0 Offset: 0x40, 0x1040			PortID: 8'h7e Device: 5 Function: 0
Bit	**Attr**	**Default**	**Description**
31:2	RW	0x0	interrupt_address: The interrupt address is interpreted as the address of any other interrupt from a PCI Express port.

6.7.12 vtd[0:1]_fltevtupraddr

Type: MEM Bus: 0 Offset: 0x44, 0x1044			PortID: 8'h7e Device: 5 Function: 0
Bit	**Attr**	**Default**	**Description**
31:0	RW	0x0	address:

6.7.13 vtd[0:1]_pmen

Intel VT-d Protect Memory Enable.

Type: MEM Bus: 0 Offset: 0x64, 0x1064			PortID: 8'h7e Device: 5 Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW	0x0	protmemen: Enable Protected Memory PROT_LOW_BASE/LIMIT and PROT_HIGH_BASE/LIMIT memory regions. Software can use the protected low/high address ranges to protect both the DMA remapping tables and the interrupt remapping tables. There is no separate set of registers provided for each.
0:0	RO_V	0x0	protregionsts: This bit is set by the processor whenever it has completed enabling the protected memory region per the rules stated in the Intel VT-d spec

6.7.14 vtd[0:1]_prot_low_mem_base

Intel VT-d Protected Memory Low Base.

Type: MEM Bus: 0 Offset: 0x68, 0x1068		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:21	RW	0x0	addr: 16 MB aligned base address of the low protected DRAM region Note that Intel VT-d engine generated reads/writes (page walk, interrupt queue, invalidation queue read, invalidation status) themselves are allowed toward this region, but no DMA accesses (non-translated DMA or ATS translated DMA or pass through DMA, that is, no DMA access of any kind) from any device is allowed toward this region (regardless of whether TE is 0 or 1), when enabled.

6.7.15 vtd[0:1]_prot_low_mem_limit

Intel VT-d Protected Memory Low Limit.

Type: MEM Bus: 0 Offset: 0x6c, 0x106c		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:21	RW	0x0	addr: 16 MB aligned limit address of the low protected DRAM region Note that Intel VT-d engine generated reads/writes (page walk, interrupt queue, invalidation queue read, invalidation status) themselves are allowed toward this region, but no DMA accesses (non-translated DMA or ATS translated DMA or pass through DMA, that is, no DMA access of any kind) from any device is allowed toward this region (regardless of whether TE is 0 or 1) when enabled.

6.7.16 vtd[0:1]_prot_high_mem_base

Intel VT-d Protected Memory High Base.

Type: MEM Bus: 0 Offset: 0x70, 0x1070		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:21	RW	0x0	addr: 16 MB aligned base address of the high protected DRAM region Note that Intel VT-d engine generated reads/writes (page walk, interrupt queue, invalidation queue read, invalidation status) themselves are allowed toward this region, but no DMA accesses (non-translated DMA or ATS translated DMA or pass through DMA, that is, no DMA access of any kind) from any device is allowed toward this region (regardless of whether TE is 0 or 1) when enabled.

6.7.17 vtd[0:1]_prot_high_mem_limit

Intel VT-d Protected Memory High Limit.

Type: MEM Bus: 0 Offset: 0x78, 0x1078		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:21	RW	0x0	addr: 16 MB aligned limit address of the high protected DRAM region Note that Intel VT-d engine generated reads/writes (page walk, interrupt queue, invalidation queue read, invalidation status) themselves are allowed toward this region, but no DMA accesses (non-translated DMA or ATS translated DMA or pass through DMA, that is, no DMA access of any kind) from any device is allowed toward this region (regardless of whether TE is 0 or 1), when enabled.

6.7.18 vtd[0:1]_inv_queue_head

Intel VT-d Invalidation Queue Header Pointer.

Type: MEM Bus: 0 Offset: 0x80, 0x1080		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
18:4	RO_V	0x0	queue_head: Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware. This field is incremented after the command has been fetched successfully and has been verified to be a valid/supported command.

6.7.19 vtd[0:1]_inv_queue_tail

Intel VT-d Invalidation Queue Tail Pointer.

Type: MEM Bus: 0 Offset: 0x88, 0x1088		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
18:4	RW	0x0	queue_tail: Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.

6.7.20 vtd[0:1]_inv_queue_add

Intel VT-d Invalidation Queue Address.

Type: MEM Bus: 0 Offset: 0x90, 0x1090		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
63:12	RW	0x0	invreq_queue_base_address: This field points to the base of size-aligned invalidation request queue.
2:0	RW	0x0	queue_size: This field specifies the length of the invalidation request queue. The number of entries in the invalidation queue is defined as 2^(X + 8) , where X is the value programmed in this field.

6.7.21 vtd[0:1]_inv_comp_status

Intel VT-d Invalidation Completion Status.

Type: MEM Bus: 0 Offset: 0x9c, 0x109c		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
0:0	RW1CS	0x0	invalidation_wait_descriptor_complete: Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field set. Hardware clears this field whenever it is executing a wait descriptor with IF field set and sets this bit when the descriptor is complete.

6.7.22 nonisoch_inv_cmp_evtctrl

Invalidation Completion Event Control.

Type: MEM Bus: 0 Offset: 0xa0		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:31	RW	0x1	inval_nonisoch_msgmsk: 0: No masking of interrupt. When a invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values). 1: This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.

Type: MEM Bus: 0 Offset: 0xa0		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
30:30	RO_V	0x0	inval_nonisoch_msi_pend: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as:- An Invalidation Wait Descriptor with Interrupt Flag (IF) field set completed, setting the IWC field in the Fault Status register. - If the IWC field in the Invalidation Event Status register was already set at the time of setting this field, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: (a) Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field. (b) Software servicing the IWC field in the Fault Status register.
29:0	RO	0x0	inval_nonisoch_msgmsk_const:

6.7.23 nonisoch_invevtdata

Invalidation Event Data.

Type: MEM Bus: 0 Offset: 0xa4		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:16	RO	0x0	inval_nonisoch_data_const:
15:0	RW	0x0	inval_nonisoch_data:

6.7.24 vtd[0:1]_inv_comp_evt_addr

Intel VT-d Invalidation Completion Event Address.

Type: MEM Bus: 0 Offset: 0xa8, 0x10a8		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:2	RW	0x0	interrupt_address:

6.7.25 vtd[0:1]_inv_comp_evt_upraddr

Type: MEM Bus: 0 Offset: 0xac, 0x10ac		PortID: 8'h7e Device: 5	Function: 0
Bit	**Attr**	**Default**	**Description**
31:0	RW	0x0	address:

6.7.26 vtd[0:1]_intr_remap_table_base

Intel VT-d Interrupt Remapping Table Based Address.

Type: MEM Bus: 0 Offset: 0xb8, 0x10b8	PortID: 8'h7e Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
63:12	RW	0x0	intr_remap_base: This field points to the base of page-aligned interrupt remapping table. If the Interrupt Remapping Table is larger than 4 KB in size, it must be size-aligned. Reads of this field returns value that was last programmed to it.
11:11	RW	0x0	ia32_extended_interrupt_enable: 0: IA32 system is operating in legacy IA32 interrupt mode. Hardware interprets only 8-bit APICID in the Interrupt Remapping Table entries. 1: IA32 system is operating in extended IA32 interrupt mode. Hardware interprets 32-bit APICID in the Interrupt Remapping Table entries.
3:0	RW	0x0	size: This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2^(X+1), where X is the value programmed in this field.

6.7.27 vtd0_fltrec[0:7]_gpa, vtd1_fltrec0_gpa

Intel VT-d Fault Record.

Type: MEM Bus: 0 Offset: vtd0: 0x110, 0x120, 0x130, 0x140, 0x150, 0x160, 0x170 vtd1: 0x1100	PortID: 8'h7e Device: 5	Function: 0	
Bit	**Attr**	**Default**	**Description**
63:12	ROS_V	0x0	gpa: 4K aligned GPA for the faulting transaction. valid only when F field is set.

6.7.28 vtd0_fltrec[0:7]_src, vtd1_fltrec0_src

Intel VT-d Fault Record.

Type: MEM	PortID: 8'h7e		
Bus: 0	Device: 5	Function: 0	
Offset: vtd0: 0x108, 0x118, 0x128, 0x138, 0x148, 0x158, 0x168, 0x178 vtd1: 0x1108			

Bit	Attr	Default	Description
63:63	RW1CS	0x0	f: Fault. Hardware sets this field to indicate a fault is logged in this fault recording register. The F field is set by hardware after the details of the fault is recorded in the PADDR, SID, FR and T fields.When this field is set, hardware may collapse additional faults from the same requestor (SID). Software writes the value read from this field to clear it.
62:62	ROS_V	0x0	type: Type of the first faulted DMA request 0: DMA write 1: DMA read request This field is only valid when Fault (F) bit is set.
61:60	ROS_V	0x0	address_type: This field captures the AT field from the faulted DMA request. This field is valid only when the F field is set.
39:32	ROS_V	0x0	fault_reason: Reason for the first translation fault. See Intel VT-d spec for details.This field is only valid when Fault bit is set.
15:0	ROS_V	0x0	source_identifier: Requester ID of the dma request that faulted. Valid only when F bit is set

6.7.29 vtd[0:1]_invaddrreg

Intel VT-d Invalidate Address.

Type: MEM	PortID: 8'h7e	
Bus: 0	Device: 5	Function: 0
Offset: 0x200, 0x1200		

Bit	Attr	Default	Description
63:12	RW	0x0	addr: To request a page-specific invalidation request to hardware, software must first write the corresponding guest physical address to this register, and then issue a page-specific invalidate command through the IOTLB_REG.
6:6	RW	0x0	ih: The field provides hint to hardware to preserve or flush the respective non-leaf page-table entries that may be cached in hardware. 0: Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, IIO must flush both the cached leaf and nonleaf page-table entries corresponding to mappings specified by ADDR and AM fields. IIO performs a domain-level invalidation on non-leaf entries and page-selective-domain-level invalidation at the leaf level. 1: Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, IIO preserves the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields and performs only a page-selective invalidation at the leaf level.
5:0	RW	0x0	am: IIO supports values of 0-9. All other values result in undefined results.

6.7.30 vtd[0:1]_iotlbinv

Intel VT-d IOTLB Invalidate.

Type: MEM **Bus:** 0 **Offset:** 0x208, 0x1208	**PortID:** 8'h7e **Device:** 5	**Function:** 0	

Bit	Attr	Default	Description
63:63	RW_V	0x0	Intel VT: Invalidate IOTLB cache Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field. Hardware clears the Intel VT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must read back and check the CPU field to be clear to confirm the invalidation is complete. When CPU field is set, software must not update the contents of this register (and Invalidate Address register, if it is being used), nor submit new IOTLB invalidation requests.
61:60	RW	0x0	iirg: IOTLB Invalidation Request Granularity When requesting hardware to invalidate the I/OTLB (by setting the Intel VT field), software writes the requested invalidation granularity through this IIRG field. Following are the encoding for the 2-bit IIRG field. 00: Reserved. Hardware ignores the invalidation request and reports invalidation complete by clearing the Intel VT field and reporting 00 in the AIG field. 01: Global Invalidation request. 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. 11: Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, the domain-id must be provided in the DID field.
58:57	RO_V	0x0	iaig: IOTLB Actual Invalidation Granularity Hardware reports the granularity at which an invalidation request was proceed through the AIG field at the time of reporting invalidation completion (by clearing the Intel VT field). The following are the encoding for the 2-bit IAIG field. 00: Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests or an unsupported/undefined encoding in IIRG. 01: Global Invalidation performed. The processor sets this in response to a global IOTLB invalidation request. 10: Domain-selective invalidation performed using the domain-id that was specified by software in the DID field. The processor sets this in response to a domain selective IOTLB invalidation request. 11: CPU sets this in response to a page selective invalidation request.
49:49	RW	0x0	dr: CPU uses this to drain or not drain reads on an invalidation request.
48:48	RW	0x0	dw: CPU uses this to drain or not drain reads on an invalidation request.
47:32	RW	0x0	did: Domain to be invalidated and is programmed by software for both page and domain selective invalidation requests. CPU ignores the bits 47:40 since it supports only an 8 bit Domain ID.

6.8 Memhot

6.8.1 vid

Type: CFG Bus: 0 Offset: 0x0		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x8086	vendor_identification_number: The value is assigned by PCI-SIG to Intel.

6.8.2 did

Type: CFG Bus: 0 Offset: 0x2		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x2f29	device_identification_number: Device ID values vary from function to function.

6.8.3 pcicmd

Type: CFG Bus: 0 Offset: 0x4		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
10:10	RW	0x0	intx_interrupt_disable:

6.8.4 pcists

Type: CFG Bus: 0 Offset: 0x6		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
4:4	RO	0x1	capl:
3:3	RO_V	0x1	intxstat:

6.8.5 rid

Type: CFG Bus: 0 Offset: 0x8		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register in any Intel® Xeon® Processor E7 v4 product family function. Implementation Note: Read and write requests from the host to any RID register in any Intel® Xeon® Processor E7 v4 product family function are re-directed to the IIO cluster. Accesses to the CCR field are also redirected due to DWORD alignment. It is possible that JTAG accesses are direct, so will not always be redirected.

6.8.6 ccr

Type: CFG Bus: 0 Offset: 0x9		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
23:16	RO	0x8	base_class: Generic Device
15:8	RO	0x80	sub_class: Generic Device
7:0	RO	0x0	interface:

6.8.7 clsr

Type: CFG Bus: 0 Offset: 0xc		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	cacheline_size: This register is set as RW for compatibility reasons only. Cacheline size is always 64B.

6.8.8 plat

Type: CFG Bus: 0 Offset: 0xd		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	primary_latency_timer: Not applicable to PCI Express. Hardwired to 00h.

6.8.9 hdr

Type: CFG Bus: 0 Offset: 0xe		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:7	RO	0x0	multi_function_device: This bit defaults to 1b since all these devices are multi-function
6:0	RO	0x0	configuration_layout: This field identifies the format of the configuration header layout. It is Type 0 for all these devices. The default is 00h, indicating a 'endpoint device'.

6.8.10 bist

Type: CFG Bus: 0 Offset: 0xf		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	bist_tests: Not supported. Hardwired to 00h

6.8.11 svid

Type: CFG Bus: 0 Offset: 0x2c		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x0	subsystem_vendor_identification_number: The default value specifies Intel but can be set to any value once after reset.

6.8.12 sdid

Type: CFG Bus: 0 Offset: 0x2e		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x0	subsystem_device_identification_number: Assigned by the subsystem vendor to uniquely identify the subsystem

6.8.13 capptr

Type: CFG Bus: 0 Offset: 0x34		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x40	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.

6.8.14 intl

Type: CFG Bus: 0 Offset: 0x3c		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	interrupt_line: NA for these devices

6.8.15 intpin

Type: CFG Bus: 0 Offset: 0x3d		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	interrupt_pin: NA since these devices do not generate any interrupt on their own

6.8.16 mingnt

Type: CFG Bus: 0 Offset: 0x3e	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	mgv:

6.8.17 maxlat

Type: CFG Bus: 0 Offset: 0x3f	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	mlv:

6.8.18 pxpcap

Type: CFG Bus: 0 Offset: 0x40e	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
29:25	RO	0x0	interrupt_message_number: NA for this device
24:24	RO	0x0	slot_implemented: NA for integrated endpoints
23:20	RO	0x9	device_port_type: Device type is Root Complex Integrated Endpoint
19:16	RO	0x1	capability_version: PCI Express Capability is Compliant with Version 1.0 of the PCI Express Spec. ***Note:*** This capability structure is not compliant with Versions beyond 1.0, since they require additional capability registers to be reserved. The only purpose for this capability structure is to make enhanced configuration space available. Minimizing the size of this structure is accomplished by reporting version 1.0 compliancy and reporting that this is an integrated root port device. As such, only three Dwords of configuration space are required for this structure.
15:8	RO	0x80	next_ptr: Pointer to the next capability. Set to 0 to indicate there are no more capability structures.
7:0	RO	0x10	capability_id: Provides the PCI Express capability ID assigned by PCI-SIG.

6.8.19 msicap

MSI Capability.

Type: CFG Bus: 0 Offset: 0x80		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:8	RO	0x0	next_ptr: Next pointer. 0: There are no other capability structures in the lower config space
7:0	RO	0x5	capability_id: 05 for MSI capability.

6.8.20 msictl

MSI Control.

Type: CFG Bus: 0 Offset: 0x82		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:9	RV	0x0	Reserved
8:8	RO	0x0	pvmc: Per Vector Masking Capable. This function does not support per vector masking.
7:7	RO	0x1	b64ac: 64 bit Address Capable. This function is 64 bit address capable.
6:4	RO	0x0	mme: Multiple Message Enable. This function only supports one vector.
3:1	RO	0x0	mmc: Multiple Message Capable. This function only requests one vector.
0:0	RW	0x0	msien: MSI Enable. Enables MSI's from this function if set. If cleared, then this function will generate legacy interrupts.

6.8.21 msiar

The MSI Address Register MSIAR contains the system specific address information to route MSI interrupts from the root ports and is broken into its constituent fields.

Type: CFG Bus: 0 Offset: 0x84		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
63:2	RW	0x0	msi_address: MSI Address. (DWORD aligned
1:0	RV	0x0	Reserved

6.8.22 msidr

MSI Data.

Type: CFG Bus: 0 Offset: 0x8c		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
15:0	RW	0x0	msidr_data: Message Data.

6.8.23 memhpctrl

Memory Hot-Plug Control.

Type: CFG Bus: 0 Offset: 0xa0		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
31:1	RV	0x0	Reserved
0:0	RW	0x0	smien: Intel SMI Enable. Enable Intel SMI interrupt generation on any hotplug event (regardless of whether it is enabled in the MemHP capabilities).

6.8.24 xpprivc1

Type: CFG Bus: 0 Offset: 0xd0		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
5:5	RWS	0x0	hpmsiclapsen:
4:4	RWS	0x1	hpmsirevalen:

6.8.25 memhpcap[0:3]

Channel X Memory Hot-Plug Capability (X = 0, 1, 2, 3)

Type: CFG Bus: 0 Offset: 0x100, 0x110, 0x120, 0x130		PortID: N/A Device: 5	Function: 1
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x110 (memhpcap0) 0x120 (memhpcap1) 0x130 (memhpcap2) 0x0 (memhpcap3)	next_ptr: Next Pointer. This points to the next capability structure.
19:16	RO	0x1	capability_version:
15:0	RO	0xb	vendor_specific_capability:

6.8.26 memhphdr[0:3]

Channel X Memory Hot-Plug Capability Header. (X = 0, 1, 2, 3)

Type: CFG Bus: 0 Offset: 0x104, 0x114, 0x124, x134	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
31:20	RO	0x10	vendor_specific_length: There are 16 bytes in this capability structure.
19:16	RO	0x1	vendor_specific_revision_id: First revision of this capability structure.
15:0	RO	0x6	vendor_specific_id: Represents the Memory Hotplug Capability.

6.8.27 sltcap[0:3]

Channel X Slot Capability (X=0, 1, 2, 3)

Type: CFG Bus: 0 Offset: 0x108, 0x118, 0x128, 0x138	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
31:19	RW_O	0x0	physical_slot_number: Indicates the associated memory channel number.
18:18	RO	0x0	command_complete_not_capable: If set, indicates that this structure is not capable of generating an interrupt on completion of the last command.
17:17	RW-O	0x0	electromechanical_interlock_present: This bit when set indicates that an Electromechanical Interlock is implemented on the chassis for this slot and that lock is controlled by bit 11 in Slot Control register. This field is initialized by BIOS based on the system architecture. BIOS note: this capability is not set if the Electromechanical Interlock control is connected to main slot power control. This is expected to be used only for hot-pluggable slots.
16:7	RV	0x0	Reserved
6:6	RW_O	0x0	hot_plug_capable: This field defines hot-plug support capabilities for the Memory Channel 0: indicates that this slot is not capable of supporting Hot-plug operations. 1: indicates that this slot is capable of supporting Hot-plug operations This bit is programmed by BIOS based on the system design. This bit must be programmed by BIOS to be consistent with the VPP enable bit for the port.
5:5	RO	0x0	hot_plug_surprise: This field indicates that a device in this slot may be removed from the system without prior notification. This field is initialized by BIOS. 0: indicates that hot-plug surprise is not supported 1: indicates that hot-plug surprise is supported This bit is not set because there are no known usage models and no hardware mechanism for detecting a surprise hotplug event.

Type: CFG	PortID: N/A		
Bus: 0	Device: 5	Function: 1	
Offset: 0x108, 0x118, 0x128, 0x138			

Bit	Attr	Default	Description
4:4	RW_O	0x0	power_indicator_present: This bit indicates that a Power Indicator is implemented for this slot and is electrically controlled by the chassis. 0: indicates that a Power Indicator that is electrically controlled by the chassis is not present 1: indicates that Power Indicator that is electrically controlled by the chassis is present BIOS programs this field.
3:3	RW_O	0x0	attention_indicator_present: This bit indicates that an Attention Indicator is implemented for this slot and is electrically controlled by the chassis 0: indicates that an Attention Indicator that is electrically controlled by the chassis is not present 1: indicates that an Attention Indicator that is electrically controlled by the chassis is present BIOS programs this field.
2:2	RW_O	0x0	mrl_sensor_present: This bit indicates that an MRL Sensor is implemented on the chassis for this slot. 0: indicates that an MRL Sensor is not present 1: indicates that an MRL Sensor is present BIOS programs this field.
1:1	RW_O	0x0	power_controller_present: This bit indicates that a software controllable power controller is implemented on the chassis for this slot. 0: indicates that a software controllable power controller is not present 1: indicates that a software controllable power controller is present BIOS programs this field.
0:0	RW_O	0x0	attention_button_present: This bit indicates that the Attention Button event signal is routed (from slot or on-board in the chassis) to the IIO's hotplug controller. 0: indicates that an Attention Button signal is not routed to IIO 1: indicates that an Attention Button is routed to IIO BIOS programs this field.

6.8.28 sltcon[0:3]

Channel X Slot Control (X=0, 1, 2, 3)

Type: CFG	PortID: N/A		
Bus: 0	Device: 5	Function: 1	
Offset: 0x10c, 0x11c, 0x12c, 0x13c			

Bit	Attr	Default	Description
15:12	RV	0x0	Reserved
11:11	RWS	0x0	electromechanical_interlock_control: When software writes a 1 to this bit, IIO pulses the EMIL pin. Write of 0 has no effect. This bit always returns a 0 when read. If electromechanical lock is not implemented, then either a write of 1 or 0 to this register has no effect.

Type: CFG	PortID: N/A		
Bus: 0	Device: 5	Function: 1	
Offset: 0x10c, 0x11c, 0x12c, 0x13c			

Bit	Attr	Default	Description
10:10	RWS	0x1	power_controller_control: If a power controller is implemented, when writes to this field will set the power state of the slot as indicated by this bit. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 0: Power On 1: Power Off
9:8	RW	0x3	power_indicator_control: If a Power Indicator is implemented, writes to this field will set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00: Reserved 01: On 10: Blink (IIO drives 1 Hz square wave for Chassis mounted LEDs) 11: Off
7:6	RW	0x3	attention_indicator_control: If an Attention Indicator is implemented, writes to this field will set the Attention Indicator to the written state. Reads of this field reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00: Reserved 01: On 10: Blink (IIO drives 1 Hz square wave) 11: Off
5:5	RW	0x0	hot_plug_interrupt_enable: When set to 1b, this bit enables generation of Hot-Plug interrupt, MSI or INTx interrupt depending on the setting of the MSI enable bit in 'MSI Control Register (MSICTRL)' on enabled Hot-Plug events. 0: Disables interrupt generation on Hot-plug events 1: Enables interrupt generation on Hot-plug events
4:4	RW	0x0	command_completed_interrupt_enable: This field enables software notification (Interrupt - MSI/INTx) when a command is completed by the Hot-plug controller connected to the PCI Express port 0: Disables hot-plug interrupts on a command completion by a hot-plug Controller 1: Enables hot-plug interrupts on a command completion by a hot-plug Controller
3:3	RW	0x0	presence_detect_changed_enable: This bit enables the generation of hot-plug interrupts or wake messages via a presence detect changed event. 0: Disables generation of hot-plug interrupts when a presence detect changed event happens. 1: Enables generation of hot-plug interrupts when a presence detect changed event happens.
2:2	RW	0x0	mrl_sensor_changed_enable: This bit enables the generation of hot-plug interrupts or wake messages via a MRL Sensor changed event. 0: Disables generation of hot-plug interrupts when an MRL Sensor changed event happens. 1: Enables generation of hot-plug interrupts when an MRL Sensor changed event happens.

Type: CFG Bus: 0 Offset: 0x10c, 0x11c, 0x12c, 0x13c	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
1:1	RW	0x0	power_fault_detected_enable: This bit enables the generation of hot-plug interrupts or wake messages via a power fault event. 0: Disables generation of hot-plug interrupts when a power fault event happens. 1: Enables generation of hot-plug interrupts when a power fault event happens.
0:0	RW	0x0	attention_button_pressed_enable: This bit enables the generation of hot-plug interrupts or wake messages via an attention button pressed event. 0: Disables generation of hot-plug interrupts when the attention button is pressed. 1: Enables generation of hot-plug interrupts when the attention button is pressed.

6.8.29 sltsts[0:3]

Channel X Slot Status. (X=0, 1, 2, 3)

Type: CFG Bus: 0 Offset: 0x10e, 0x11e, 0x12e, 0x13e	PortID: N/A Device: 5	Function: 1	
Bit	**Attr**	**Default**	**Description**
15:8	RV	0x0	Reserved
7:7	RO	0x0	electromechanical_latch_status: When read this register returns the current state of the Electromechanical Interlock (the EMILS pin) which has the defined encodings as: 0: Electromechanical Interlock Disengaged 1: Electromechanical Interlock Engaged
6:6	RO	0x0	presence_detect_state: When read, this register returns the current state of the Present Detect pin. 0: Module slot empty 1: Module Present in slot (powered or unpowered)
5:5	RO	0x0	mrl_sensor_state: This bit reports the status of an MRL sensor if it is implemented. 0: MRL Closed 1: MRL Open
4:4	RW1C	0x0	command_completed: This bit is set by IIO when the hot-plug command has completed and the hot-plug controller is ready to accept a subsequent command. It is subsequently cleared by software after the field has been read and processed. This bit provides no guarantee that the action corresponding to the command is complete. Any write to SLTCON (regardless of the port is capable or enabled for hot-plug) is considered a 'hot-plug' command. If the port is not hot-plug capable or hot-plug enabled, then the hot-plug command does not trigger any action on the VPP port but the command is still completed via this bit.
3:3	RW1C	0x0	presence_detect_changed: This bit is set by IIO when the value reported in bit 6 is changes. It is subsequently cleared by software after the field has been read and processed.
2:2	RW1C	0x0	mrl_sensor_changed: This bit is set if the value reported in bit 5 changes. It is subsequently cleared by software after the field has been read and processed.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 1
Offset: 0x10e, 0x11e, 0x12e, 0x13e		

Bit	Attr	Default	Description
1:1	RW1C	0x0	power_fault_detected: This bit is set by IIO when a power fault event is detected by the power controller (which is reported via the VPP bit stream). It is subsequently cleared by software after the field has been read and processed.
0:0	RW1C	0x0	attention_button_pressed: This bit is set by IIO when the attention button is pressed. It is subsequently cleared by software after the field has been read and processed.

6.9 Device 5 Function 2

Global System Control and Error Registers.

Register Name	Offset	Size
vid	0x0	16
did	0x2	16
pcicmd	0x4	16
pcists	0x6	16
rid	0x8	8
ccr	0x9	24
clsr	0xc	8
hdr	0xe	8
svid	0x2c	16
sdid	0x2e	16
capptr	0x34	8
intl	0x3c	8
intpin	0x3d	8
pxpcapid	0x40	8
pxpnxtptr	0x41	8
pxpcap	0x42	16
irpperrsv	0x80	64
iioerrsv	0x8c	32
mierrsv	0x90	32
pcierrsv	0x94	32
sysmap	0x9c	32
viral	0xa0	32
vppctl	0xb0	64
vppsts	0xb8	32
vppfreq	0xbc	32
vppmem	0xc0	64
gcerrst	0x1a8	32
gcferrst	0x1ac	32
gcnerrst	0x1b8	32

Register Name	Offset	Size
gnerrst	0x1c0	32
gferrst	0x1c4	32
gerrctl	0x1c8	32
gsysst	0x1cc	32
gsysctl	0x1d0	32
gfferrst	0x1dc	32
gfnerrst	0x1e8	32
gnferrst	0x1ec	32
gnnerrst	0x1f8	32
irpp0errst	0x230	32
irpp0errctl	0x234	32
irpp0fferrst	0x238	32
irpp0fnerrst	0x23c	32
irpp0fferrhd0	0x240	32
irpp0fferrhd1	0x244	32
irpp0fferrhd2	0x248	32
irpp0fferrhd3	0x24c	32
irpp0nferrst	0x250	32
irpp0nnerrst	0x254	32
irpp0nferrhd0	0x258	32
irpp0nferrhd1	0x25c	32
irpp0nferrhd2	0x260	32
irpp0nferrhd3	0x264	32
irpp0errcntsel	0x268	32
irpp0errcnt	0x26c	32
irpp1errst	0x2b0	32
irpp1errctl	0x2b4	32
irpp1fferrst	0x2b8	32
irpp1fnerrst	0x2bc	32
irpp1fferrhd0	0x2c0	32
irpp1fferrhd1	0x2c4	32
irpp1fferrhd2	0x2c8	32
irpp1fferrhd3	0x2cc	32
irpp1nferrst	0x2d0	32
irpp1nnerrst	0x2d4	32
irpp1nferrhd0	0x2d8	32
irpp1nferrhd1	0x2dc	32
irpp1nferrhd2	0x2e0	32
irpp1nferrhd3	0x2e4	32
irpp1errcntsel	0x2e8	32
irpp1errcnt	0x2ec	32
iioerrst	0x300	32
iioerrctl	0x304	32

Register Name	Offset	Size
iiofferrst	0x308	32
iiofferrhd_0	0x30c	32
iiofferrhd_1	0x310	32
iiofferrhd_2	0x314	32
iiofferrhd_3	0x318	32
iiofnerrst	0x31c	32
iionferrst	0x320	32
iionferrhd_0	0x324	32
iionferrhd_1	0x328	32
iionferrhd_2	0x32c	32
iionferrhd_3	0x330	32
iionnerrst	0x334	32
iioerrcntsel	0x33c	32
iioerrcnt	0x340	32
mierrst	0x380	32
mierrctl	0x384	32
mifferrst	0x388	32
mifferrhdr_0	0x38c	32
mifferrhdr_1	0x390	32
mifferrhdr_2	0x394	32
mifferrhdr_3	0x398	32
mifnerrst	0x39c	32
minferrst	0x3a0	32
minferrhdr_0	0x3a4	32
minferrhdr_1	0x3a8	32
minferrhdr_2	0x3ac	32
minferrhdr_3	0x3b0	32
minnerrst	0x3b4	32
mierrcntsel	0x3bc	32
mierrcnt	0x3c0	8

6.9.1 vid

Type: CFG Bus: 0 Offset: 0x0	PortID: N/A Device: 5	 Function: 2	
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x8086	vendor_identification_number: The value is assigned by PCI-SIG to Intel.

6.9.2 did

Type: CFG Bus: 0 Offset: 0x2		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x2f2a	device_identification_number: Device ID values vary from function to function.

6.9.3 pcicmd

Type: CFG Bus: 0 Offset: 0x4		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
10:10	RO	0x0	intx_disable: NA for these devices
9:9	RO	0x0	fast_back_to_back_enable: Not applicable to PCI Express and is hardwired to 0
8:8	RO	0x0	serr_enable: This bit has no impact on error reporting from these devices
7:7	RO	0x0	idsel_stepping_wait_cycle_control: Not applicable to internal devices. Hardwired to 0.
6:6	RO	0x0	parity_error_response: This bit has no impact on error reporting from these devices
5:5	RO	0x0	vga_palette_snoop_enable: Not applicable to internal devices. Hardwired to 0.
4:4	RO	0x0	memory_write_and_invalidate_enable: Not applicable to internal devices. Hardwired to 0.
3:3	RO	0x0	special_cycle_enable: Not applicable. Hardwired to 0.
2:2	RO	0x0	bus_master_enable: Hardwired to 0 since these devices don't generate any transactions
1:1	RO	0x0	memory_space_enable: Hardwired to 0 since these devices don't decode any memory BARs
0:0	RO	0x0	io_space_enable: Hardwired to 0 since these devices don't decode any IO BARs

6.9.4 pcists

Type: CFG Bus: 0 Offset: 0x6		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
15:15	RO	0x0	detected_parity_error: This bit is set when the device receives a packet on the primary side with an uncorrectable data error including a packet with poison bit set or an uncorrectable addresscontrol parity error. The setting of this bit is regardless of the Parity Error Response bit PERRE in the PCICMD register.

Type: CFG	PortID: N/A		
Bus: 0	Device: 5	Function: 2	
Offset: 0x6			
Bit	**Attr**	**Default**	**Description**
14:14	RO	0x0	signaled_system_error: Hardwired to 0
13:13	RO	0x0	received_master_abort: Hardwired to 0
12:12	RO	0x0	received_target_abort: Hardwired to 0
11:11	RO	0x0	signaled_target_abort: Hardwired to 0
10:9	RO	0x0	devsel_timing: Not applicable to PCI Express. Hardwired to 0.
8:8	RO	0x0	master_data_parity_error: Hardwired to 0
7:7	RO	0x0	fast_back_to_back: Not applicable to PCI Express. Hardwired to 0.
5:5	RO	0x0	pci66mhz_capable: Not applicable to PCI Express. Hardwired to 0.
4:4	RO	0x1	capabilities_list: This bit indicates the presence of a capabilities list structure
3:3	RO	0x0	intx_status: Hardwired to 0

6.9.5 rid

Type: CFG	PortID: N/A		
Bus: 0	Device: 5	Function: 2	
Offset: 0x8			
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register in any Intel® Xeon® Processor E7 v4 product family function.

6.9.6 ccr

Type: CFG	PortID: N/A		
Bus: 0	Device: 5	Function: 2	
Offset: 0x9			
Bit	**Attr**	**Default**	**Description**
23:16	RO_V	0x8	base_class: Generic Device
15:8	RO_V	0x80	sub_class: Generic Device
7:0	RO_V	0x0	register_level_programming_interface: Set to 00h for all non-APIC devices.

6.9.7 clsr

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0xc		

Bit	Attr	Default	Description
7:0	RW	0x0	cacheline_size: This register is set as RW for compatibility reasons only. Cacheline size is always 64B.

6.9.8 hdr

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0xe		

Bit	Attr	Default	Description
7:7	RO	0x1	multi_function_device: This bit defaults to 1b since all these devices are multi-function.
6:0	RO	0x0	configuration_layout: This field identifies the format of the configuration header layout. It is Type 0 for all these devices. The default is 00h, indicating a 'endpoint device'.

6.9.9 svid

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x2c		

Bit	Attr	Default	Description
15:0	RW_O	0x0	subsystem_vendor_identification_number: The default value specifies Intel but can be set to any value once after reset.

6.9.10 sdid

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x2e		

Bit	Attr	Default	Description
15:0	RW_O	0x0	subsystem_device_identification_number: Assigned by the subsystem vendor to uniquely identify the subsystem.

6.9.11 capptr

Type: CFG Bus: 0 Offset: 0x34		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x40	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.

6.9.12 intl

Type: CFG Bus: 0 Offset: 0x3c		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	interrupt_line: NA for these devices

6.9.13 intpin

Type: CFG Bus: 0 Offset: 0x3d		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	interrupt_pin: NA since these devices do not generate any interrupt on their own.

6.9.14 pxpcapid

Type: CFG Bus: 0 Offset: 0x40		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x10	capability_id: Provides the PCI Express capability ID assigned by PCI-SIG.

6.9.15 pxpnxtptr

Type: CFG Bus: 0 Offset: 0x41		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	next_ptr: This field is set to the PCI Power Management capability.

6.9.16 pxpcap

Type: CFG Bus: 0 Offset: 0x42		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
13:9	RO	0x0	interrupt_message_number_n_a:
8:8	RO	0x0	slot_implemented_n_a:
7:4	RO	0x9	device_port_type: This field identifies the type of device. It is set to for the DMA to indicate root complex integrated endpoint device.
3:0	RO	0x2	capability_version: This field identifies the version of the PCI Express capability structure. Set to 2h for PCI Express and DMA devices for compliance with the extended base registers.

6.9.17 irpperrsv

IRP Protocol Error Severity.

Type: CFG Bus: 0 Offset: 0x80		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
29:28	RWS	0x2	protocol_parity_error: (DB) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
27:26	RWS	0x2	protocol_qt_overflow_underflow: (DA) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
21:20	RWS	0x2	protocol_rcvd_unexprsp: (D7) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
9:8	RWS	0x1	csr_acc_32b_unaligned: (C3) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
7:6	RWS	0x1	wrcache_uncecc_error: (C2) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
5:4	RWS	0x1	protocol_rcvd_poison: (C1) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved

Type: CFG Bus: 0 Offset: 0x80		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
3:2	RWS	0x0	wrcache_correcc_error: (B4) 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved

6.9.18 iioerrsv

IIO Core Error Severity.

This register associates the detected IIO internal core errors to an error severity level. An individual error is reported with the corresponding severity in this register. Software can program the error severity to one of the three severities supported by IIO. This register is sticky and can only be reset by PWRGOOD.

Type: CFG Bus: 0 Offset: 0x8c		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
13:12	RWS_L	0x1	c6_overflow_underflow_error: 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
9:8	RWS_L	0x1	c4_master_abort_address_error: 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved
1:0	RWS_L	0x0	c7_multicast_target_error: Multicast target error, indicating a MCAST transaction has targeted more than the number of groups supported. 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved

6.9.19 mierrsv

Miscellaneous Error Severity.

Type: CFG Bus: 0 Offset: 0x90		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:6	RWS	0x0	vpp_err_sts: 00: Error Severity Level 0 (Correctable) 01: Error Severity Level 1 (Recoverable) 10: Error Severity Level 2 (Fatal) 11: Reserved This bit should be programmed to 1.

6.9.20 pcierrsv

PCIe Error Severity Map.

This register allows remapping of the PCIe errors to the IIO error severity.

Type: CFG Bus: 0 Offset: 0x94		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
5:4	RWS	0x2	pciefaterr_map: 10: Map this PCIe error type to Error Severity 2 01: Map this PCIe error type to Error Severity 1 00: Map this PCIe error type to Error Severity 0
3:2	RWS	0x1	pcienonfaterr_map: 10: Map this PCIe error type to Error Severity 2 01: Map this PCIe error type to Error Severity 1 00: Map this PCIe error type to Error Severity 0
1:0	RWS	0x0	pciecorerr_map: 10: Map this PCIe error type to Error Severity 2 01: Map this PCIe error type to Error Severity 1 00: Map this PCIe error type to Error Severity 0

6.9.21 sysmap

System Error Event map.

This register maps the error severity detected by the IIO to one of the system events. When an error is detected by the IIO, its corresponding error severity determines which system event to generate according to this register.

Type: CFG Bus: 0 Offset: 0x9c		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
10:8	RWS	0x1	sev2_map: 010: Generate NMI 001: Generate Intel SMI/PMI 000: No inband message Others: Reserved
6:4	RWS	0x2	sev1_map: 010: Generate NMI 001: Generate SMIPMI 000: No inband message Others: Reserved
2:0	RWS	0x0	sev0_map: 010: Generate NMI 001: Generate SMIPMI 000: No inband message Others: Reserved

6.9.22 viral

This register provides the option to generate viral alert upon the detection of fatal error.

Type: CFG Bus: 0 Offset: 0xa0		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
31:31	RW1C	0x0	iio_viral_state: Indicates the IIO cluster is in a viral state. When set, all outbound requests are master aborted, all inbound requests are master aborted. This includes traffic to and from the DMI port, except the Reset_Warn message, which will be auto-completed by the DMI port. This state bit is cleared by warm reset.
30:30	RW1CS	0x0	iio_viral_status: Indicates the IIO cluster had gone to viral. This bit has no effect on hardware and does not indicate the IIO is currently in the viral state. This bit is persistent through warm reset (sticky), even though the viral state is not.
2:2	RW	0x0	iio_global_viral_mask: 0: IIO Viral State assertion will cause IIO hardware packet blocking. 1: IIO Viral State assertion will not cause IIO hardware packet blocking.
1:1	RW	0x0	Reserved (Rsvd): Reserved
0:0	RW	0x0	iio_fatal_viral_alert_enable: Enables IIO viral alert.

6.9.23 vppctl

This register defines the control/command for PCA9555.

Type: CFG Bus: 0 Offset: 0xb0		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
63:60	RO	0x1	vpp_version: Specified the version of this structure for BIOS use. 0: VPPCTL with PCIe ports. 1: VPPCTL with 11 PCIe prots + VPPMEM with 4 memory ports.
55:55	RWS	0x0	vpp_reset_mode: 0: Power good reset will reset the VPP state machines and hard reset will cause the VPP state machine to terminate at the next 'logical' VPP stream boundary and then reset the VPP state machines 1: Both power good and hard reset will reset the VPP state machines
54:44	RWS	0x0	vpp_en: When set, the VPP function for the corresponding root port is enabled. Enable Root Port [54] Port 3d [53] Port 3c [52] Port 3b [51] Port 3a [50] Port 2d [49] Port 2c [48] Port 2b [47] Port 2a [46] Port 1b [45] Port 1a [44] Port 0 (PCIe mode only)
43:0	RWS	0x0	vpp_enaddr: Assigns the VPP address of the device on the VPP interface and assigns the port address for the ports within the VPP device. There are more address bits then root ports so assignment must be spread across VPP ports. Port Addr Root Port [40] [43:41] Port 3d [36] [39:37] Port 3c [32] [35:33] Port 3b [28] [31:29] Port 3a [24] [27:25] Port 2d [20] [23:21] Port 2c [16] [19:17] Port 2b [12] [15:13] Port 2a [8] [11:9] Port 1a [4] [7:5] Port 1a [0] [3:1] Port 0 (PCIe mode only)

6.9.24 vppsts

This register defines the status from PCA9555

Type: CFG Bus: 0 Offset: 0xb8		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
0:0	RW1CS	0x0	vpp_error: VPP Port error happened i.e. an unexpected STOP of NACK was seen on the VPP port

6.9.25 vppfreq

Type: CFG Bus: 0 Offset: 0xbc		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
31:24	RWS	0x1e	vpp_tpf: Pulse Filter should be set to 60 nS. The value used is dependent on the internal clock frequency. In this case, internal clock frequency is 500 MHz, so the default value represents 60 nS at that rate.
23:16	RWS	0x96	vpp_thd_data: Hold time for Data is 300 nS. The default value is set to 300 nS when the internal clock rate is 500 MHz.
11:0	RWS	0x9c4	vpp_tsu_thd: Represents the high time and low time of the SCL pin. It should be set to 5 uS for a 100 kHz SCL clock 5 uS high time and 5 uS low time. The default value represents 5 uS with an internal clock of 500 MHz.

6.9.26 vppmem

Type: CFG Bus: 0 Offset: 0xc0		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
63:40	RV	0x0	Reserved:
39:32	RWS	0x0	vpp_en: When set, the VPP function for the corresponding root port is enabled. Enable Root Port [39] reserved. [38] reserved. [37] reserved. [36] reserved. [35] Memory Channel x [34] Memory Channel x [33] Memory Channel x [32] Memory Channel x

Type: CFG Bus: 0 Offset: 0xc0		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
31:0	RWS	0x0	vpp_enaddr: Assigns the VPP address of the device on the VPP interface and assigns the port address for the ports within the VPP device. There are for memory channel hotplug. Port Addr Root Port [31] [30:28] Reserved [27] [27:24] Reserved [23] [22:20] Reserved [19] [18:16] Reserved [15] [14:12] Memory Channel x [11] [10:8] Memory Channel x [7] [6:4] Memory Channel x [3] [2:0] Memory Channel x

6.9.27 gcerrst

This register indicates the corrected error reported to the IIO global error logic. An individual error status bit that is set indicates that a particular local interface has detected an error.

Type: CFG Bus: 0 Offset: 0x1a8		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
26:26	RV	0x0	MC error Memory Controller Error Status.
25:25	RW	0b	Intel VT-d Error This register indicates the corrected error reported to the Intel VT-d error logic. An individual error status bit that is set indicates that a particular local interface has detected an error.
24:24	RW	0b	Miscellaneous Error
23:23	RW	0b	IIO Core Error
20:20	RW	0b	DMI Error
15:5	RW	0x0	PCIe* Error Bit 5: Port 0 Bit 6: Port 1a Bit 7: Port 1b Bit 8: Port 2a Bit 9: Port 2b Bit 10: Port 2c Bit 11: Port 2d Bit 12: Port 3a Bit 13: Port 3b Bit 14: Port 3c Bit 15: Port 3d
1:1	RW	0x0	IRP1 Error Mask
0:0	RW	0b	IRP0 Error Mask; When set, disables logging of error

6.9.28 gcferrst

Type: CFG Bus: 0 Offset: 0x1ac		Device: 5	PortID: N/A Function: 2
Bit	**Attr**	**Default**	**Description**
26:26	RV	0x0	MC error Memory Controller Error Status.
25:25	RW	0b	Intel VT-d Error
24:24	RW	0b	Miscellaneous Error
23:23	RW	0b	IIO Core Error
20:20	RW	0b	DMI Error
15:5	RW	0x0	PCIe* Error Bit 5: Port 0 Bit 6: Port 1a Bit 7: Port 1b Bit 8: Port 2a Bit 9: Port 2b Bit 10: Port 2c Bit 11: Port 2d Bit 12: Port 3a Bit 13: Port 3b Bit 14: Port 3c Bit 15: Port 3d
1:1	RW	0x0	IRP1 Error Mask
0:0	RW	0b	IRP0 Error Mask; When set, disables logging of error

6.9.29 gcnerrst

Type: CFG Bus: 0 Offset: 0x1b8			PortID: N/A Device: 5 Function: 2
Bit	**Attr**	**Default**	**Description**
26:26	RV	0x0	MC error Memory Controller Error Status.
25:25	RW	0b	Intel® VT-d Error
24:24	RW	0b	Miscellaneous Error
23:23	RW	0b	IIO Core Error
20:20	RW	0b	DMI Error
15:5	RW	0x0	PCIe* Error Bit 5: Port 0 Bit 6: Port 1a Bit 7: Port 1b Bit 8: Port 2a Bit 9: Port 2b Bit 10: Port 2c Bit 11: Port 2d Bit 12: Port 3a Bit 13: Port 3b Bit 14: Port 3c Bit 15: Port 3d
1:1	RW	0x0	IRP1 Error Mask
0:0	RW	0b	IRP0 Error Mask; When set, disables logging of error

6.9.30 gnerrst

Global Non-Fatal Error Status.

This register indicates the non-fatal error reported to the IIO global error logic. An individual error status bit that is set indicates that a particular local interface has detected an error.

Type: CFG Bus: 0 Offset: 0x1c0			PortID: N/A Device: 5 Function: 2
Bit	**Attr**	**Default**	**Description**
25:25	RW1CS	0x0	vtd: Intel VT-d Error Status This register indicates the non-fatal error reported to the Intel VT-d error logic. An individual error status bit that is set indicates that a particular local interface has detected an error.
24:24	RW1CS	0x0	mi: Miscellaneous Error Status
23:23	RW1CS	0x0	iio: IIO Core Error Status This bit indicates that IIO core has detected an error
20:20	RW1CS	0x0	dmi: This bit indicates that IIO DMI port 0 has detected an error.
15:15	RW1CS	0x0	pcie10:
14:14	RW1CS	0x0	pcie9:
13:13	RW1CS	0x0	pcie8:
12:12	RW1CS	0x0	pcie7:
11:11	RW1CS	0x0	pcie6:
10:10	RW1CS	0x0	pcie5:
9:9	RW1CS	0x0	pcie4:
8:8	RW1CS	0x0	pcie3:
7:7	RW1CS	0x0	pcie2:
6:6	RW1CS	0x0	pcie1:
5:5	RW1CS	0x0	pcie0:
3:3	RW1CS	0x0	csipro1:
2:2	RW1CS	0x0	csipro0:
1:1	RW1CS	0x0	IRP1 Coherent Interface Error
0:0	RW1CS	0x0	IRP0 Coherent Interface Error

6.9.31 gferrst

Global Fatal Error Status.

This register indicates the fatal error reported to the IIO global error logic. An individual error status bit that is set indicates that a particular local interface has detected an error.

Type: CFG Bus: 0 Offset: 0x1c4		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
25:25	RW1CS	0x0	vtd: This register indicates the fatal error reported to the Intel VT-d error logic. An individual error status bit that is set indicates that a particular local interface has detected an error.
24:24	RW1CS	0x0	mi: Miscellaneous Error Status
23:23	RW1CS	0x0	iio: IIO Core Error Status This bit indicates that IIO core has detected an error
20:20	RW1CS	0x0	dmi: This bit indicates that IIO DMI port 0 has detected an error.
15:15	RW1CS	0x0	pcie10:
14:14	RW1CS	0x0	pcie9:
13:13	RW1CS	0x0	pcie8:
12:12	RW1CS	0x0	pcie7:
11:11	RW1CS	0x0	pcie6:
10:10	RW1CS	0x0	pcie5:
9:9	RW1CS	0x0	pcie4:
8:8	RW1CS	0x0	pcie3:
7:7	RW1CS	0x0	pcie2:
6:6	RW1CS	0x0	pcie1:
5:5	RW1CS	0x0	pcie0:
1:1	RW1CS	0x0	IRP1 Coherent Interface Error::
0:0	RW1CS	0x0	IRP0 Coherent Interface Error:

6.9.32 gerrctl

Global Error Control.

This register controls/masks the reporting of errors detected by the IIO local interfaces. An individual error control bit that is set masks error reporting of the particular local interface; software may set or clear the control bit. This register is sticky and can only be reset by PWRGOOD. Note that bit fields in this register can become reserved depending on the port configuration. For example, if the PCIe port is configured as 2X8 ports, then only the corresponding PCI-EX8 bit fields are valid; other bits are unused and reserved.Global error control register masks errors reported from the local interface to the global register. If the an error reporting is disabled in this register, all errors from the corresponding local interface will not set any of the global error status bits.

Type: CFG Bus: 0 Offset: 0x1c8		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
26:26	RV	0x0	MC error Memory Controller Error Status.
25:25	RW	0x0	vtd_err_msk:
24:24	RW	0x0	mi_err_msk:
23:23	RW	0x0	iio_err_msk:
20:20	RW	0x0	dmi_err_msk: This bit enables/masks the error detected in the DMI[0] Port.
15:15	RW	0x0	pcie_err_msk10:
14:14	RW	0x0	pcie_err_msk9:
13:13	RW	0x0	pcie_err_msk8:
12:12	RW	0x0	pcie_err_msk7:
11:11	RW	0x0	pcie_err_msk6:
10:10	RW	0x0	pcie_err_msk5:
9:9	RW	0x0	pcie_err_msk4:
8:8	RW	0x0	pcie_err_msk3:
7:7	RW	0x0	pcie_err_msk2:
6:6	RW	0x0	pcie_err_msk1:
5:5	RW	0x0	pcie_err_msk0:
3:3	RW	0x0	csip_err_msk1:
2:2	RW	0x0	csip_err_msk0:
1:1	RW	0x0	IRP1 Error Mask:
0:0	RW	0x0	IRP0 Error Mask: When set, disables logging of this error

6.9.33 gsysst

Global System Event Status.

This register indicates the error severity signaled by the IIO global error logic. Setting of an individual error status bit indicates that the corresponding error severity has been detected by the IIO.

Type: CFG Bus: 0 Offset: 0x1cc		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
2:2	ROS_V	0x0	sev2: When set, IIO has detected an error of error severity 2
1:1	ROS_V	0x0	sev1: When set, IIO has detected an error of error severity 1
0:0	ROS_V	0x0	sev0: When set, IIO has detected an error of error severity 0

6.9.34 gsysctl

Global System Event Control.

The system event control register controls/masks the reporting the errors indicated by the system event status register. When cleared, the error severity does not cause the generation of the system event. When set, detection of the error severity generates system events according to system event map register (SYSMAP).

Type: CFG Bus: 0 Offset: 0x1d0		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
2:2	RW	0x0	sev2_en: When set, the detection of error severity 2 generates system events.
1:1	RW	0x0	sev1_en: When set, the detection of error severity 1 generates system events.
0:0	RW	0x0	sev0_en: When set, the detection of error severity 0 generates system events.

6.9.35 gfferrst, gfnerrst

Global Fatal FERR and NERR Status.

Type: CFG Bus: 0 Offset: 0x1dc, 0x1e8		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
26:0	ROS_V	0x0	log: This field logs the global error status register content when the first fatal error is reported. This has the same format as the global fatal error status register (GFERRST).

6.9.36 gnferrst, gnnerrst

Global Non-Fatal FERR and NERR Status

Type: CFG Bus: 0 Offset: 0x1ec, 0x1f8		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
26:0	ROS_V	0x0	log: This filed logs the global error status register content when the first non-fatal error is reported. This has the same format as the global non-fatal error status register (GNERRST).

6.9.37 irpp[0:1]errst

IRP Protocol Error Status.

This register indicates the error detected by the Coherent Interface.

Type: CFG Bus: 0 Offset: 0x230, 0x2b0		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
14:14	RW1CS	0x0	protocol_parity_error: (DB) Originally used for detecting parity error on coherent interface, however, no parity checks exist. So this logs parity errors on data from the IIO switch on the inbound path.
13:13	RW1CS	0x0	protocol_qt_overflow_underflow: (DA)
10:10	RW1CS	0x0	protocol_rcvd_unexprsp: (D7) A completion has been received from the Coherent Interface that was unexpected.
6:6	RW1CS	0x0	csr_acc_32b_unaligned: (C3)
4:4	RW1CS	0x0	wrcache_uncecc_error1: (C2) A double bit ECC error was detected within the Write Cache in set 1.
3:3	RW1CS	0x0	wrcache_uncecc_error0: (C2) A double bit ECC error was detected within the Write Cache in set 0.
3:3	RW1CS	0x0	protocol_rcvd_poison: (C1) A poisoned packet has been received from the Coherent Interface.
2:2	RW1CS	0x0	wrcache_correcc_error1: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 1.
1:1	RW1CS	0x0	wrcache_correcc_error0: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 0.

6.9.38 irpp[0:1]errctl

IRP Protocol Error Control.

This register enables the error status bit setting for a Coherent Interface detected error. Setting of the bit enables the setting of the corresponding error status bit in IRPPERRST register. If the bit is cleared, the corresponding error status will not be set.

Type: CFG Bus: 0 Offset: 0x234, 0x2b4		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
14:14	RWS	0x0	protocol_parity_error: (DB) 0: Disable error status logging for this error 1: Enable Error status logging for this error
13:13	RWS	0x0	protocol_qt_overflow_underflow: (DA) 0: Disable error status logging for this error 1: Enable Error status logging for this error
10:10	RWS	0x0	protocol_rcvd_unexprsp: (D7) 0: Disable error status logging for this error 1: Enable Error status logging for this error

Type: CFG Bus: 0 Offset: 0x234, 0x2b4		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
6:6	RWS	0x0	csr_acc_32b_unaligned: (C3) 0: Disable error status logging for this error 1: Enable Error status logging for this error
3:3	RWS	0x0	wrcache_uncecc_error1: (C2) 0: Disable error status logging for this error 1: Enable Error status logging for this error
4:4	RWS	0x0	wrcache_uncecc_error0: (C2) 0: Disable error status logging for this error 1: Enable Error status logging for this error
3:3	RWS	0x0	protocol_rcvd_poison: (C1) 0: Disable error status logging for this error 1: Enable Error status logging for this error
2:2	RWS	0x0	wrcache_correcc_error1: (B4) 0: Disable error status logging for this error 1: Enable Error status logging for this error.
1:1	RW1CS	0x0	wrcache_correcc_error0: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 0.

6.9.39 irpp[0:1]fferrst, irpp[0:1]fnerrst

IRP Protocol Fatal FERR and NERR Status.

The error status log indicates which error is causing the report of the first fatal error event.

Type: CFG Bus: 0 Offset: irp0: 0x238, 0x23c irp1: 0x2b8, 0x2bc		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
14:14	ROS_V	0x0	protocol_parity_error: (DB) Originally used for detecting parity error on coherent interface, however, no parity checks exist. So this logs parity errors on data from the IIO switch on the inbound path.
13:13	ROS_V	0x0	protocol_qt_overflow_underflow: (DC)
10:10	ROS_V	0x0	protocol_rcvd_unexprsp: (D7) A completion has been received from the Coherent Interface that was unexpected.
6:6	ROS_V	0x0	csr_acc_32b_unaligned: (C3)
4:4	ROS_V	0x0	wrcache_uncecc_error1: (C2) A double bit ECC error was detected within the Write Cache in set 1.
3:3	ROS_V	0x0	wrcache_uncecc_error0: (C2) A double bit ECC error was detected within the Write Cache in set 0.
3:3	ROS_V	0x0	protocol_rcvd_poison: (C1) A poisoned packet has been received from the Coherent Interface.
2:2	ROS_V	0x0	wrcache_correcc_error1: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 1.

Type: CFG Bus: 0 Offset: irp0: 0x238, 0x23c irp1: 0x2b8, 0x2bc	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
1:1	ROS_V	0x0	wrcache_correcc_error0: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 0.

6.9.40 irpp[0:1]fferrhd[0:3]

IRP Protocol Fatal FERR Header Log.

Type: CFG Bus: 0 Offset: irpp0fferrhd: 0x240, 0x244, 0x248, 0x24c irpp1fferrhd: 0x2c0, 0x2c4, 0x2c8, 0x2cc	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
31:0	ROS_V	0x0	hdr: Logs the respective DWORD of the header on an error condition

6.9.41 irpp[0:1]nferrst, irpp[0:1]nnerrst

IRP Protocol Non-Fatal FERR and NERR Status.

The error status log indicates which error is causing the report of the first non-fatal error event.

Type: CFG Bus: 0 Offset: irp0: 0x250, 0x254, irp1: 0x2d0, 0x2d4	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
14:14	ROS_V	0x0	protocol_parity_error: Originally used for detecting parity error on coherent interface, however, no parity checks exist. So this logs parity errors on data from the IIO switch on the inbound path.
13:13	ROS_V	0x0	protocol_qt_overflow_underflow:
10:10	ROS_V	0x0	protocol_rcvd_unexprsp: A completion has been received from the Coherent Interface that was unexpected.
6:6	ROS_V	0x0	csr_acc_32b_unaligned: (C3)
4:4	ROS_V	0x0	wrcache_uncecc_error1: (C2) A double bit ECC error was detected within the Write Cache in set 1.
3:3	ROS_V	0x0	wrcache_uncecc_error0: (C2) A double bit ECC error was detected within the Write Cache in set 0.
3:3	ROS_V	0x0	protocol_rcvd_poison: (C1) A poisoned packet has been received from the Coherent Interface.
2:2	ROS_V	0x0	wrcache_correcc_error1: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 1.

Type: CFG Bus: 0 Offset: irp0: 0x250, 0x254, irp1: 0x2d0, 0x2d4	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
1:1	ROS_V	0x0	wrcache_correcc_error0: (B4) A single bit ECC error was detected and corrected within the Write Cache in set 0.

6.9.42 irpp[0:1]nferrhd[0:3]

IRP Protocol Non-Fatal FERR Header Log.

Type: CFG Bus: 0 Offset: irpp0nferrhd: 0x258, 0x25c, 0x260, 0x264 irpp1nferrhd: 0x2d8, 0x2dc, 0x2e0, 0x2e4	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
31:0	ROS_V	0x0	hdr: Logs the respective DWORD of the header on an error condition.

6.9.43 irpp[0:1]errcntsel

IRP Protocol Error Counter Select.

Type: CFG Bus: 0 Offset: 0x268, 0x2e8	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
18:0	RW	0x0	irp_error_count_select: See IRPP0ERRST for per bit description of each error. Each bit in this field has the following behavior: 0: Do not select this error type for error counting. 1: Select this error type for error counting.

6.9.44 irpp[0:1]errcnt

IRP Protocol Error Count.

Type: CFG Bus: 0 Offset: 0x26c, 0x2ec	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
7:7	RW1CS	0x0	errovf: Error Accumulator Overflow. 0: No overflow occurred. 1: Error overflow. The error count may not be valid.

Type: CFG Bus: 0 Offset: 0x26c, 0x2ec		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
6:0	RW1CS	0x0	errcnt: This counter accumulates errors that occur when the associated error type is selected in the ERRCNTSEL register. ***Notes:*** This register is cleared by writing 7Fh. Maximum counter available is 7Fh

6.9.45 iioerrst

IIO Core Error Status.

This register indicates the IIO internal core errors detected by the IIO error logic. An individual error status bit that is set indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit. This register is sticky and can only be reset by PWRGOOD. Clearing of the IIOERRST is done by clearing the corresponding IIOERRST bits.

Type: CFG Bus: 0 Offset: 0x300		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
6:6	RW1CS	0x0	c6: Overflow/Underflow Error Status (C6)
4:4	RW1CS	0x0	c4: Master Abort Error Status (C4)
0:0	RW1CS	0x0	c7_multicast_target_error: Multicast target error indicating a multicast transaction has targeted more than the number of groups supported.

6.9.46 iioerrctl

IIO Core Error Control.

This register controls the reporting of IIO internal core errors detected by the IIO error logic. An individual error control bit that is cleared masks reporting of that a particular error; software may set or clear the respective bit. This register is sticky and can only be reset by PWRGOOD.

Type: CFG Bus: 0 Offset: 0x304		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
8:8	RWS_L	0x0	c4_inbound_ler_disable: Disable logging C4 error due to the PCIe being down due to being in LER mode. ***Note:*** Locked by RSPLCK

Type: CFG Bus: 0 Offset: 0x304		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
7:7	RWS_L	0x0	c4_outbound_ler_disable: Disable logging C4 error due to the PCIe being down due to being in LER mode. ***Note:*** Locked by RSPLCK
6:6	RWS_L	0x0	c6: Overflow/Underflow Error Enable (C6)
4:4	RWS_L	0x0	c4: Master Abort Error Enable (C4)
0:0	RWS_L	0x0	c7_multicast_target_error — Multicast Target Error Enable.

6.9.47 iiofferrst, iiofnerrst

IIO Core Fatal FERR and NERR Status.

Type: CFG Bus: 0 Offset: 0x308, 0x31c		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
6:0	ROS_V	0x0	iio_core_error_status_log: The error status log indicates which error is causing the report of the first error event. The encoding indicates the corresponding bit position of the error in the error status register. It has the same field mapping as IIOERRST.

6.9.48 iiofferrhd_[0:3]

IIO Core Fatal FERR Header.

Type: CFG Bus: 0 Offset: 0x30c, 0x310, 0x314, 0x318		PortID: N/A Device: 5	Function: 2
Bit	**Attr**	**Default**	**Description**
31:0	ROS_V	0x0	iio_core_error_header_log: Logs the respective DWORD of the header on an error condition.

6.9.49 iionferrst, iionnerrst

IIO Core Non-Fatal FERR and NERR Status.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x320, 0x334		

Bit	Attr	Default	Description
6:0	ROS_V	0x0	iio_core_error_status_log: The error status log indicates which error is causing the report of the first error event. The encoding indicates the corresponding bit position of the error in the error status register. It has the same field mapping as IIOERRST.

6.9.50 iionferrhd_[0:3]

IIO Core Non-Fatal FERR Header.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x324, 0x328, 0x32c, 0x330		

Bit	Attr	Default	Description
31:0	ROS_V	0x0	iio_core_error_header_log: Logs the respective DWORD of the header on an error condition. Header log stores the IIO data path header information of the associated IIO core error. The header indicates where the error is originating from and the address of the cycle.

6.9.51 iioerrcntsel

IIO Core Error Counter Selection.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x33c		

Bit	Attr	Default	Description
6:6	RW_L	0x0	c6: Overflow/Underflow Error Count Select
4:4	RW_L	0x0	c4: Master Abort Error Select
1:1	RW_L	0x0	c7_multicast_target_error: Multicast Target Error Select

6.9.52 iioerrcnt

IIO Core Error Counter.

Type: CFG Bus: 0 Offset: 0x340	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
7:7	RW1CS	0x0	errovf: 0: No overflow occurred 1: Error overflow. The error count may not be valid.
6:0	RW1CS	0x0	errcnt: This counter accumulates errors that occur when the associated error type is selected in the ERRCNTSEL register. Notes: This register is cleared by writing 7Fh. Maximum counter available is 7Fh.

6.9.53 mierrst

Miscellaneous Error Status.

Type: CFG Bus: 0 Offset: 0x380	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
3:3	RW1CS	0x0	vpp_err_sts: VPP Hotplug I/O Extender Port Error Status. I/O module encountered persistent VPP failure. The VPP is unable to operate.

6.9.54 mierrctl

Miscellaneous Error Control.

Type: CFG Bus: 0 Offset: 0x384	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
3:3	RWS	0x0	vpp_err_sts: VPP Error Status Enable.

6.9.55 mifferrst, mifnerrst

Miscellaneous Fatal FERR and NERR Status.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x388, 0x39c		

Bit	Attr	Default	Description
10:0	ROS_V	0x0	mi_err_st_log: There is 1 bit per VPP port to support up to 11 slots. This field only logs VPP errors. Vpp is serial bus that indicates which port (slot) has a hot plug event pending.

6.9.56 mifferrhdr_[0:3]

Miscellaneous Fatal FERR Header Log.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x38c, 0x390, 0x394, 0x398		

Bit	Attr	Default	Description
31:0	ROS_V	0x0	hdr: Logs the respective DWORD of the header on an error condition.

6.9.57 minferrst, minnerrst

Miscellaneous Non-Fatal FERR and NERR Status.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x3a0, 0x3b4		

Bit	Attr	Default	Description
10:0	ROS_V	0x0	mi_err_st_log: There is 1 bit per VPP port to support up to 11 slots. This field only logs VPP errors. Vpp is serial bus that indicates which port (slot) has a hot plug event pending.

6.9.58 minferrhdr_[0:3]

Miscellaneous Non-Fatal FERR Header Log.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 2
Offset: 0x3a4, 0x3a8, 0x3ac, 0x3b0		

Bit	Attr	Default	Description
31:0	ROS_V	0x0	hdr: Logs the respective DWORD of the header on an error condition.

6.9.59 mierrcntsel

Miscellaneous Error Count Select.

Type: CFG Bus: 0 Offset: 0x3bc	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
3:3	RW	0x0	vpp_err_sts: VPP Error Status Count Select.

6.9.60 mierrcnt

Miscellaneous Error Count.

Type: CFG Bus: 0 Offset: 0x3c0	PortID: N/A Device: 5	Function: 2	
Bit	**Attr**	**Default**	**Description**
7:7	RW1CS	0x0	errovflow: 0: No overflow occurred 1: Error overflow. The error count may not be valid.
6:0	RW1CS	0x0	errcnt: This counter accumulates errors that occur when the associated error type is selected in the ERRCNTSEL register. Notes: This register is cleared by writing 7Fh. Maximum counter available is 127d (7Fh).

6.10 Device 5 Function 4

I/OxAPCI Configuration Space.

Register Name	Offset	Size
vid	0x0	16
did	0x2	16
pcicmd	0x4	16
pcists	0x6	16
rid	0x8	8
ccr	0x9	24
clsr	0xc	8
hdr	0xe	8
mbar	0x10	32
svid	0x2c	16
sid	0x2e	16
capptr	0x34	8
intlin	0x3c	8
intpin	0x3d	8

Register Name	Offset	Size
abar	0x40	16
pxpcap	0x44	32
snapshot_index	0x80	8
snapshot_window	0x90	32
ioapictetpc	0xa0	32
pmcap	0xe0	32
pmcsr	0xe4	32
ioadsels0	0x288	32
iointsrc0	0x2a0	32
iointsrc1	0x2a4	32
ioremintcnt	0x2a8	32
ioremgpecnt	0x2ac	32
FauxGV	0x2c4	32

6.10.1 vid

Type: CFG Bus: 0 Offset: 0x0	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x8086	vendor_identification_number:

6.10.2 did

Type: CFG Bus: 0 Offset: 0x2	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x2f2c	device_identification_number:

6.10.3 pcicmd

Type: CFG Bus: 0 Offset: 0x4	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
10:10	RO	0x0	intxdisable:
9:9	RO	0x0	fb2be:
8:8	RO	0x0	serre:
7:7	RO	0x0	idsel:
6:6	RO	0x0	perrrsp:
5:5	RO	0x0	vga:

Type: CFG Bus: 0 Offset: 0x4		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
4:4	RO	0x0	memwrinv:
3:3	RO	0x0	spcen:
2:2	RW	0x0	bme:
1:1	RW	0x0	mse:
0:0	RO	0x0	iose:

6.10.4 pcists

Type: CFG Bus: 0 Offset: 0x6		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
15:15	RO_V	0x0	dpe:
14:14	RO	0x0	sse:
13:13	RO	0x0	rma:
12:12	RO	0x0	rta:
11:11	RW1C	0x0	sta:
10:9	RO	0x0	devselt:
8:8	RO	0x0	medierr:
7:7	RO	0x0	fb2bcap:
5:5	RO	0x0	sixtysixmhzcap:
4:4	RO	0x1	capl:
3:3	RO	0x0	intxst:

6.10.5 rid

Type: CFG Bus: 0 Offset: 0x8		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register in any Intel® Xeon® Processor E7 v4 product family function.

6.10.6 ccr

Type: CFG Bus: 0 Offset: 0x9	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
23:16	RO_V	0x80	base_class: Generic Device
15:8	RO_V	0x0	sub_class: Generic Device
7:0	RO_V	0x20	interface:

6.10.7 clsr

Type: CFG Bus: 0 Offset: 0xc	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	clsr_reg:

6.10.8 hdr

Type: CFG Bus: 0 Offset: 0xe	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
7:7	RO	0x1	multi_function_device: This bit defaults to 1b since all these devices are multi-function.
6:0	RO	0x0	configuration_layout: This field identifies the format of the configuration header layout. It is Type 0 for all these devices. The default is 00h, indicating a 'endpoint device'.

6.10.9 mbar

I/OxAPIC Based Address.

Type: CFG Bus: 0 Offset: 0x10	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
31:12	RW	0x0	bar: This marks the 4 KB aligned 32-bit base address for memory-mapped registers of I/OxAPICSide note: Any accesses via message channel or JTAG mini port to registers pointed to by the MBAR address, are not gated by MSE bit (in PCICMD register) being set, that is, even if MSE bit is a 0, message channel accesses to the registers pointed to by MBAR address are allowed completed normally. These accesses are accesses from internal ucode/ microcode and JTAG and they are allowed to access the registers normally even if this bit is clear.

Type: CFG Bus: 0 Offset: 0x10	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
3:3	RO	0x0	prefetchable: The I/OxAPIC registers are not prefetchable.
2:1	RO	0x0	type: The IOAPIC registers can only be placed below 4G system address space.
0:0	RO	0x0	memory_space: This Base Address Register indicates memory space.

6.10.10 svid

Type: CFG Bus: 0 Offset: 0x2c	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x8086	svid_reg: The default value specifies Intel but can be set to any value once after reset.

6.10.11 sid

This value is used to identify a particular subsystem.

Type: CFG Bus: 0 Offset: 0x2e	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
15:0	RW_O	0x0	sid_reg: Assigned by the subsystem vendor to uniquely identify the subsystem.

6.10.12 capptr

Type: CFG Bus: 0 Offset: 0x34	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x44	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.

6.10.13 intlin

Type: CFG Bus: 0 Offset: 0x3c	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	intlin_reg:

6.10.14 intpin

Type: CFG Bus: 0 Offset: 0x3d	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x0	intpin_reg:

6.10.15 abar

I/OxAPIC Alternate BAR.

Type: CFG Bus: 0 Offset: 0x40	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
15:15	RW	0x0	abar_enable: When set, the range FECX_YZ00 to FECX_YZFF is enabled as an alternate access method to the I/OxAPIC registers and these addresses are claimed by the IIO's internal I/OxAPIC regardless of the setting the MSE bit in the IOxAPIC config space. Bits 'XYZ' are defined below.
11:8	RW	0x0	base_address_19: 16 (XBAD) These bits determine the high order bits of the I/O APIC address map. When a memory address is recognized by the IIO which matches FECX_YZ00-to-FECX_YZFF, the IIO will respond to the cycle and access the internal I/O APIC.
7:4	RW	0x0	base_address_15: 12 (YBAD) These bits determine the low order bits of the IO APIC address map. When a memory address is recognized by the IIO which matches FECX_YZ00-to-FECX_YZFF, the IIO will respond to the cycle and access the internal I/O APIC.
3:0	RW	0x0	base_address_11: 8 (ZBAD) These bits determine the low order bits of the I/O APIC address map. When a memory address is recognized by the IIO which matches FECX_YZ00-to-FECX_YZFF, the IIO will respond to the cycle and access the internal I/O APIC.

6.10.16 pxpcap

Type: CFG Bus: 0 Offset: 0x44		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
29:25	RO	0x0	interrupt_message_numnber:
24:24	RO	0x0	slot_implemented:
23:20	RO	0x9	device_port_type: Device type is Root Complex Integrated Endpoint
19:16	RO	0x1	capability_version: PCI Express Capability is Compliant with Version 1.0 of the PCI Express Spec. ***Note:*** This capability structure is not compliant with Versions beyond 1.0, since they require additional capability registers to be reserved. The only purpose for this capability structure is to make enhanced configuration space available. Minimizing the size of this structure is accomplished by reporting version 1.0 compliancy and reporting that this is an integrated root port device. As such, only three Dwords of configuration space are required for this structure.
15:8	RO	0xe0	next_ptr: Pointer to the next capability. Set to 0 to indicate there are no more capability structures, else default value.
7:0	RO	0x10	capability_idat: Provides the PCI Express capability ID assigned by PCI-SIG.

6.10.17 snapshot_index

Type: CFG Bus: 0 Offset: 0x80		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	ssidx: When PECI/JTAG wants to read the indirect RTE registers of I/OxAPIC, this register is used to point to the index of the indirect register, as defined in the I/ OxAPIC indirect memory space. Software writes to this register and then does a read of the RDWINDOW register to read the contents at that index. Note h/w does not preclude software from accessing this register over the coherent interface but that is not what this register is defined for.

6.10.18 snapshot_window

Type: CFG Bus: 0 Offset: 0x90		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
31:0	RO_V	0x0	sswindow: When SMBUS/JTAG reads this register, the data contained in the indirect register pointed to by the RDINDEX register is returned on the read.

6.10.19 ioapictetpc

Type: CFG Bus: 0 Offset: 0xa0		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
10:10	RW	0x0	port3c_intb: 0: srcint is connected to IOAPIC table entry 21 1: srcint is connected to IOAPIC table entry 19
8:8	RW	0x0	port3a_intb: 0: srcint is connected to IOAPIC table entry 20 1: srcint is connected to IOAPIC table entry 17
6:6	RW	0x0	port2c_intb: 0: srcint is connected to IOAPIC table entry 13 1: srcint is connected to IOAPIC table entry 11
4:4	RW	0x0	port2a_intb: 0: srcint is connected to IOAPIC table entry 12 1: srcint is connected to IOAPIC table entry 9
0:0	RW	0x0	port0_intb: 0: srcint is connected to IOAPIC table entry 1 1: srcint is connected to IOAPIC table entry 3

6.10.20 pmcap

Power Management Capabilities.

Type: CFG Bus: 0 Offset: 0xe0		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
31:27	RO	0x0	pme_support: Bits 31, 30 and 27 must be set to '1' for PCI-PCI bridge structures representing ports on root complexes.
26:26	RO	0x0	d2_support: I/OxAPIC does not support power management state D2
25:25	RO	0x0	d1_support: I/OxAPIC does not support power management state D1
24:22	RO	0x0	aux_current:
21:21	RO	0x0	device_specific_initalization:
19:19	RO	0x0	pme_clock: This field is hardwired to 0h as it does not apply to PCI Express.
18:16	RW_O	0x3	version: This field is set to 3h (Power Management 1.2 compliant) as version number. Bit is RW-O to make the version 2h incase legacy OS'es have any issues.
15:8	RO	0x0	next_pointer: This is the last capability in the chain and hence set to 0.
7:0	RO	0x1	capability_id: Provides the Power Management capability ID assigned by PCI-SIG.

6.10.21 pmcsr

Power Management Control and Status.

Type: CFG	PortID: N/A	
Bus: 0	Device: 5	Function: 4
Offset: 0xe4		

Bit	Attr	Default	Description
31:24	RO	0x0	data: Not relevant for I/OxAPIC
23:23	RO	0x0	bpcce: Not relevant for I/OxAPIC
22:22	RO	0x0	b2b3: Not relevant for I/OxAPIC
15:15	RO	0x0	pmests: Not relevant for I/OxAPIC
14:13	RO	0x0	dscl: Not relevant for I/OxAPIC
12:9	RO	0x0	dsel: Not relevant for I/OxAPIC
8:8	RO	0x0	pmeen: Not relevant for I/OxAPIC
3:3	RO	0x1	rstd3hotd0: Indicates I/OxAPIC does not reset its registers when transitioning from D3hot to D0.
1:0	RW_V	0x0	power_state: This 2-bit field is used to determine the current power state of the function and to set a new power state as well. 00: D0 01: D1 (not supported by IOAPIC) 10: D2 (not supported by IOAPIC) 11: D3_hot If Software tries to write 01 or 10 to this field, the power state does not change from the existing power state (which is either D0 or D3hot) and nor do these bits1:0 change value. When in D3hot state, I/OxAPIC will a) Respond to only Type 0 configuration transactions targeted at the device's configuration space, when in D3hot state. c) Will not respond to memory (that is, D3hot state is equivalent to MSE), accesses to MBAR region (note: ABAR region access still go through in D3hot state, if it enabled). d) Will not generate any MSI writes .

6.10.22 ioadsels0

I/OxAPIC DSELS Register 0.

Type: CFG Bus: 0 Offset: 0x288		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
28:28	RWS	0x0	sw2ipc_aer_negedge_msk: SW2IPC AER Negative Edge Mask
27:27	RWS	0x0	sw2ipc_aer_event_sel: SW2IPC AER Event Select

6.10.23 iointsrc0

IO Interrupt Source Register 0.

Type: CFG Bus: 0 Offset: 0x2a0		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
31:0	RW_V	0x0	int_src0: bit interrupt source 31: INTD Port 3b 30: INTC Port 3b 29: INTB Port 3b 28: INTA Port 3b 27: INTD Port 3a 26: INTC Port 3a 25: INTB Port 3a 24: INTA Port 3a 23: INTD Port 1b 22: INTC Port 1b 21: INTB Port 1b 20: INTA Port 1b 19: INTD Port 1a 18: INTC Port 1a 17: INTB Port 1a 16: INTA Port 1a 15: INTD Port 2d 14: INTC Port 2d 13: INTB Port 2d 12: INTA Port 2d 11: INTD Port 2c 10: INTC Port 2c 9: INTB Port 2c 8: INTA Port 2c 7: INTD Port 2b 6: INTC Port 2b 5: INTB Port 2b 4: INTA Port 2b 3: INTD Port 2a 2: INTC Port 2a 1: INTB Port 2a 0: INTA Port 2a

6.10.24 iointsrc1

IO Interrupt Source Register 1.

Type: CFG Bus: 0 Offset: 0x2a4		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
20:0	RW_V	0x0	int_src1: bit interrupt source 20: INTA Root Port Core 19: INTB ME KT 18: INTC ME IDE-R 17: INTD ME HECI 16: INTA ME HECI 15: INTD Intel QuickData Technology DMA 14: INTC Intel QuickData Technology DMA 13: INTB Intel QuickData Technology DMA 12: INTA Intel QuickData Technology DMA 11: INTD Port 0 DMI 10: INTC Port 0 DMI 9: INTB Port 0 DMI 8: INTA Port 0 DMI 7: INTD Port 3d 6: INTC Port 3d 5: INTB Port 3d 4: INTA Port 3d 3: INTD Port 3c 2: INTC Port 3c 1: INTB Port 3c 0: INTA Port 3c

6.10.25 ioremintcnt

Remote IO Interrupt Count.

Type: CFG Bus: 0 Offset: 0x2a8		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
31:0	RW_V	0x0	rem_int_cnt: Number of remote interrupts received.

6.10.26 ioremgpecnt

Rmote IO GPE Count.

Type: CFG Bus: 0 Offset: 0x2ac	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
23:16	RW_V	0x0	hpgpe_cnt: Number of remote HPGPEs received.
15:8	RW_V	0x0	pmgpe_cnt: Number of remote PMGPEs received.
7:0	RW_V	0x0	gpe_cnt: Number of remote GPEs received.

6.10.27 FauxGV

Type: CFG Bus: 0 Offset: 0x2c4	PortID: N/A Device: 5	Function: 4	
Bit	**Attr**	**Default**	**Description**
0:0	RWS_L	0x0	FauxGVEn: Enable Fault GV.

6.11 Device 5 Function 4 I/OxAPIC

I/OxAPIC has a direct memory mapped space. An index/data register pair is located within the directed memory mapped region and is used to access the redirection table entries. The offsets shown in the table are from the base address in either ABAR or MBAR or both.

Access to addresses beyond 0x40h return all 0s.

Only addresses up to offset 0xFF can be accessed via the ABAR register whereas offsets up to 0xFFF can be accessed via MBAR.

Only aligned DWORD reads and write are allowed towards the I/OxAPIC memory space. Any other accesses will result in an error.

Register Name	Offset	Size
index	0x0	8
window	0x10	32
eoi	0x40	8

6.11.1 index

The Index Register will select which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Type: MEM Bus: 0 Offset: 0x0		PortID: 8’h7e Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
7:0	RW_L	0x0	idx: Indirect register to access.

6.11.2 window

Type: MEM Bus: 0 Offset: 0x10		PortID: 8’h7e Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
31:0	RW_LV	0x0	window_reg: Data to be written to the indirect registers on writes, and location of read data from the indirect register on reads.

6.11.3 eoi

Type: MEM Bus: 0 Offset: 0x40		PortID: 8’h7e Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
7:0	RW_L	0x0	eoi_reg: The EOI register is present to provide a mechanism to efficiently convert level interrupts to edge triggered MSI interrupts. When a write is issued to this register, the I/O(x)APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared. Note that if multiple I/O Redirection entries, for any reason, assign the same vector, each of those entries will have the Remote_IRR bit reset to ’0’. This will cause the corresponding I/OxAPIC entries to resample their level interrupt inputs and if they are still asserted, cause more MSI interrupt(s) (if unmasked) which will again set the Remote_IRR bit.

6.12 Device 5 Function 4 Window 0

Register Name	Offset	Size
arbid__window	0x2	32
bcfg__window	0x3	32
rtl0__window	0x10	32
rth0__window	0x11	32
rtl1__window	0x12	32
rth1__window	0x13	32
rtl2__window	0x14	32
rth2__window	0x15	32
rtl3__window	0x16	32

Register Name	Offset	Size
rth3__window	0x17	32
rtl4__window	0x18	32
rth4__window	0x19	32
rtl5__window	0x1a	32
rth5__window	0x1b	32
rtl6__window	0x1c	32
rth6__window	0x1d	32
rtl7__window	0x1e	32
rth7__window	0x1f	32
rtl8__window	0x20	32
rth8__window	0x21	32
rtl9__window	0x22	32
rth9__window	0x23	32
rtl10__window	0x24	32
rth10__window	0x25	32
rtl11__window	0x26	32
rth11__window	0x27	32
rtl12__window	0x28	32
rth12__window	0x29	32
rtl13__window	0x2a	32
rth13__window	0x2b	32
rtl14__window	0x2c	32
rth14__window	0x2d	32
rtl15__window	0x2e	32
rth15__window	0x2f	32
rtl16__window	0x30	32
rth16__window	0x31	32
rtl17__window	0x32	32
rth17__window	0x33	32
rtl18__window	0x34	32
rth18__window	0x35	32
rtl19__window	0x36	32
rth19__window	0x37	32
rtl20__window	0x38	32
rth20__window	0x39	32
rtl21__window	0x3a	32
rth21__window	0x3b	32
rtl22__window	0x3c	32
rth22__window	0x3d	32
rtl23__window	0x3e	32
rth23__window	0x3f	32

6.12.0.1 arbid__window

Tracks the APICID register for compatibility reasons.

Type: MEM Bus: 0 Offset: 0x2		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
27:24	RO	0x0	arbitration_id: Tracks the APICID register.

6.12.0.2 bcfg__window

Type: MEM Bus: 0 Offset: 0x3		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
0:0	RW	0x1	boot_configuration: This bit is a default1 to indicate FSB delivery mode. A value of 0 has no effect. Its left as RW for software compatibility.

6.12.0.3 rtl[0:23]__window

The information in this register along with Redirection Table High DWORD register is used to construct the MSI interrupt. There is one of these pairs of registers for every interrupt. The first interrupt has the redirection registers at offset 10h. The second interrupt at 12h, third at 14h, etc. until the final interrupt (interrupt 23) at 3Eh.

Type: MEM Bus: 0 Offset: 0x10, 0x12, 0x14, 0x16, 0x18, 0x1a, 0x1c, 0x1e, 0x20, 0x22, 0x24, 0x26, 0x28, 0x2a, 0x2c, 0x2e, 0x30, 0x32, 0x34, 0x36, 0x38, 0x3a, 0x3c, 0x3e		PortID: N/A Device: 5	Function: 4
Bit	**Attr**	**Default**	**Description**
17:17	RW	0x0	disable_flushing: This bit has no meaning in IIO. This bit is R/W for software compatibility reasons.

Type: MEM	PortID: N/A		
Bus: 0	Device: 5	Function: 4	
Offset: 0x10, 0x12, 0x14, 0x16, 0x18, 0x1a, 0x1c, 0x1e, 0x20, 0x22, 0x24, 0x26, 0x28, 0x2a, 0x2c, 0x2e, 0x30, 0x32, 0x34, 0x36, 0x38, 0x3a, 0x3c, 0x3e			

Bit	Attr	Default	Description
16:16	RW	0x1	msk: When cleared, an edge assertion or level (depending on bit 15 in this register) on the corresponding interrupt input results in delivery of an MSI interrupt using the contents of the corresponding redirection table high/low entry. When set, an edge or level on the corresponding interrupt input does not cause MSI Interrupts and no MSI interrupts are held pending as well (i.e. if an edge interrupt asserted when the mask bit is set, no MSI interrupt is sent and the hardware does not remember the event to cause an MSI later when the mask is cleared). When set, assertion/deassertion of the corresponding interrupt input causes Assert/Deassert_INTx messages to be sent to the legacy PCH, provided the 'Disable PCI INTx Routing to PCH' bit is clear. If the latter is set, Assert/Deassert_INTx messages are not sent to the legacy PCH. When mask bit goes from 1 to 0 for an entry and the entry is programmed for level input, the input is sampled and if asserted, an MSI is sent. Also, if an Assert_INTx message was previously sent to the legacy PCH/internal-coalescing logic on behalf of the entry, when the mask bit is clear, then a Deassert_INTx event is scheduled on behalf of the entry (whether this event results in a Deassert_INTx message to the legacy PCH depends on whether there were other outstanding Deassert_INTx messages from other sources). When the mask bit goes from 0 to 1, and the corresponding interrupt input is already asserted, an Assert_INTx event is scheduled on behalf of the entry. Note though that if the interrupt is deasserted when the bit transitions from 0 to 1, a Deassert_INTx is not scheduled on behalf of the entry.
15:15	RW	0x0	tm: This field indicates the type of signal on the interrupt input that triggers an interrupt. 0 indicates edge sensitive, 1 indicates level sensitive.
14:14	RO	0x0	rirr: This bit is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. For level triggered interrupts, this bit is set when an MSI interrupt has been issued by the I/OxAPIC into the system fabric (noting that if BME bit is clear or when the mask bit is set, no new MSI interrupts cannot be generated and this bit cannot transition from 0 to 1 in those conditions). It is reset (if set) when an EOI message is received from a local APIC with the appropriate vector number, at which time the level interrupt input corresponding to the entry is resampled causing one more MSI interrupt (if other enable bits are set) and causing this bit to be set again.
13:13	RW	0x0	ip: 0=active high; 1=active low. This bit has no meaning in IIO since the Assert/Deassert_INTx messages are level in-sensitive. The OS is expected to program a 1 into this register and so the 'internal' virtual wire signals in the IIO need to be active low (i.e. 0=asserted and 1=deasserted).
12:12	RO	0x0	delivery_status: When trigger mode is set to level and the entry is unmasked, this bit indicates the state of the level interrupt i.e. 1b if interrupt is asserted else 0b. When the trigger mode is set to level but the entry is masked, this bit is always 0b. This bit is always 0b when trigger mode is set to edge.
11:11	RW	0x0	dstm: 0 - Physical 1 - Logical

Type: MEM	PortID: N/A		
Bus: 0	Device: 5	Function: 4	
Offset: 0x10, 0x12, 0x14, 0x16, 0x18, 0x1a, 0x1c, 0x1e, 0x20, 0x22, 0x24, 0x26, 0x28, 0x2a, 0x2c, 0x2e, 0x30, 0x32, 0x34, 0x36, 0x38, 0x3a, 0x3c, 0x3e			
Bit	**Attr**	**Default**	**Description**
10:8	RW	0x0	delm: This field specifies how the APICs listed in the destination field should act upon reception of the interrupt. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. The encodings are: 000 - Fixed: Trigger Mode can be edge or level. Examine TM bit to determine. 001 - Lowest Priority: Trigger Mode can be edge or level. Examine TM bit to determine. 010 - Intel SMI/PMI: Trigger mode is always edge and TM bit is ignored. 011 - Reserved 100 - NMI. Trigger mode is always edge and TM bit is ignored. 101 - INIT. Trigger mode is always edge and TM bit is ignored. 110 - Reserved 111 - ExtINT. Trigger mode is always edge and TM bit is ignored.
7:0	RW	0x0	vct: This field contains the interrupt vector for this interrupt

6.12.0.4 rth[0:23]__window

Type: MEM	PortID: N/A		
Bus: 0	Device: 5	Function: 4	
Offset: 0x11, 0x13, 0x15, 0x17, 0x19, 0x1b, 0x1d, 0x1f, 0x21, 0x23, 0x25, 0x27, 0x29, 0x2b, 0x2d, 0x2f, 0x31, 0x33, 0x35, 0x37, 0x39, 0x3b, 0x3d, 0x3f			
Bit	**Attr**	**Default**	**Description**
31:24	RW	0x0	did: They are bits [19:12] of the MSI address.
23:16	RW	0x0	edid: These bits become bits [11:4] of the MSI address.

6.13 Device 6-7 Function 0,1,3

Register Name	Offset	Size	Device 6 Function	Device 7 Function
rx_ctle_peak_gen2	0xA78	64	0,1,3	0
rx_ctle_peak_gen3	0xA80	64	1,3	0

6.13.1 rx_ctle_peak_gen2

This register controls the Continuous Time Linear Equalizer (CTLE) setting for the named receiver bundles on the selected port on the PCIe interface in Gen. 2 mode.

Type: CFG Bus: 0 Offset: 0xA78		PortID: N/A Device: 6	Function: 0
Bit	**Attr**	**Default**	**Description**
7:4	RWS_L	0x7	bndl1:
3:0	RWS_L	0x7	bndl0:

6.13.2 rx_ctle_peak_gen2

This register controls the Continuous Time Linear Equalizer (CTLE) setting for the named receiver bundles on the selected port on the PCIe interface in Gen. 2 mode.

Type: CFG Bus: 0 Offset: 0xA78		PortID: N/A Device: 6	Function: 1
Bit	**Attr**	**Default**	**Description**
15:12	RWS_L	0x7	bndl3:
11:8	RWS_L	0x7	bndl2:
7:4	RWS_L	0x7	bndl1:
3:0	RWS_L	0x7	bndl0:

6.13.3 rx_ctle_peak_gen3

This register controls the Continuous Time Linear Equalizer (CTLE) setting for the named receiver bundles on the selected port on the PCIe interface in Gen. 3 mode.

Type: CFG Bus: 0 Offset: 0xA80		PortID: N/A Device: 6	Function: 1
Bit	**Attr**	**Default**	**Description**
19:15	RWS_L	0x7	bndl3:
14:10	RWS_L	0x7	bndl2:
9:5	RWS_L	0x7	bndl1:
4:0	RWS_L	0x7	bndl0:

6.13.4 rx_ctle_peak_gen2

This register controls the Continuous Time Linear Equalizer (CTLE) setting for the named receiver bundles on the selected port on the PCIe interface in Gen. 2 mode.

Type: CFG Bus: 0 Bus: 0 Offset: 0xA78		PortID: N/A Device: 6 Device: 7	Function: 3 Function: 0
Bit	**Attr**	**Default**	**Description**
41:37	RWS_L	0x7	bndl7:
36:32	RWS_L	0x7	bndl6:
29:25	RWS_L	0x7	bndl5:
24:20	RWS_L	0x7	bndl4:
19:15	RWS_L	0x7	bndl3
14:10	RWS_L	0x7	bndl2
9:5	RWS_L	0x7	bndl1
4:0	RWS_L	0x7	bndl0

6.13.5 rx_ctle_peak_gen3

This register controls the Continuous Time Linear Equalizer (CTLE) setting for the named receiver bundles on the selected port on the PCIe interface in Gen. 3 mode.

Type: CFG Bus: 0 Bus: 0 Offset: 0xA80		PortID: N/A Device: 6 Device: 7	Function: 3 Function: 0
Bit	**Attr**	**Default**	**Description**
41:37	RWS_L	0x7	bndl7
36:32	RWS_L	0x7	bndl6
29:25	RWS_L	0x7	bndl5
24:20	RWS_L	0x7	bndl4
19:15	RWS_L	0x7	bndl3
14:10	RWS_L	0x7	bndl2
9:5	RWS_L	0x7	bndl1
4:0	RWS_L	0x7	bndl0

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