Overview of the Ethernet SPAs

This chapter provides an overview of the release history, and feature and Management Information Base (MIB) support for the Fast Ethernet, Gigabit Ethernet, and Ten Gigabit Ethernet SPAs on the Cisco ASR 1000 Series Aggregation Services Router.

This chapter includes the following sections:

- Release History, page 9-2
- Supported Features, page 9-2
- SPA Architecture, page 9-10
- Displaying the SPA Hardware Type, page 9-11

Release History

Release	Modification
Cisco IOS XE Release 3.8.0S	Added support for the Minimal Disruptive Restartfeature to the line cards that use the following Gigabit Ethernet SPAs: • SPA-2X1GE-V2 • SPA-5X1GE-V2 • SPA-8X1GE-V2 • SPA-10X1GE-V2 • SPA-1X10GE-L-V2
Cisco IOS XE Release 3.3.0S	Added support for the 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA on the Cisco ASR 1000 Series Aggregation Services Routers.
Cisco IOS XE Release 3.2	Added support for the 2-Port Gigabit Synchronous Ethernet SPA on the Cisco ASR 1000 Series Aggregation Services Router.
Cisco IOS XE Release 2.5	The maximum number of supported 802.1Q VLANs per Ethernet SPA was increased with the **hw-module subslot ethernet vlan unlimited** global configuration command.
Cisco IOS XE Release 3.1.0S	Information pertaining to change in **show running-config interface Fast Ethernet** *slot/subslot/port* command output for 4-Port Fast Ethernet SPA was added.
Cisco IOS XE Release 2.1	First release. Support for the following SPAs was introduced on the Cisco ASR1000-SIP10 on the Cisco ASR 1000 Series Aggregation Services Routers: **Fast Ethernet SPAs** • 4-Port FastEthernet SPA • 8-Port Fast Ethernet SPA **Gigabit Ethernet SPAs** • 10-Port Gigabit Ethernet SPA, Version 2 • 8-Port Gigabit Ethernet SPA, Version 2 • 5-Port Gigabit Ethernet SPA, Version 2 • 2-Port Gigabit Ethernet SPA, Version 2 • 1-Port 10-Gigabit Ethernet SPA, Version 2

Supported Features

The following is a list of some of the significant hardware and software features supported by Gigabit Ethernet SPAs and 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA on the Cisco ASR 1000 Series Aggregation Services Routers:

- Autonegotiation. 1-Port 10 Gigabit Ethernet LAN/WAN PHY SPA does not support autonegotiation.
- Auto-MDI/MDIX detection. The SFP-GE-T module enables auto-MDI/MDIX detection on the 5-Port, 8-Port, and 10-Port Gigabit Ethernet SPAs and also on the Built-in Gigabit Ethernet Ports for the Cisco ASR 1000 Series Aggregation Services Routers.

- Full-duplex operation
- 802.1Q VLAN termination
- Jumbo frames support (9216 bytes)
- Support for command-line interface (CLI)-controlled OIR
- 802.3x flow control
- The following maximum number of VLANs per SPA:
  - Up to 8100 VLANs per SPA—For all Ethernet SPAs supported on the Cisco ASR 1000 Series Aggregation Services Routers in software releases prior to Cisco IOS XE Release 2.5.
  - Up to 4094 VLANs per port per SPA—For all Ethernet SPAs supported on the Cisco ASR 1000 Series Aggregation Services Routers beginning in Cisco IOS XE Release 2.5 using the **hw-module subslot ethernet vlan unlimited** command.
- Up to 5000 MAC Accounting Entries per SPA (Source MAC Accounting on the ingress and Destination MAC Accounting on the egress)
- Per-port byte and packet counters for policy drops, oversubscription drops, CRC error drops, packet sizes, unicast, multicast, and broadcast packets
- Per-VLAN byte and packet counters for policy drops, oversubscription drops, unicast, multicast, and broadcast packets
- Per-port byte counters for good bytes and dropped bytes
- Multiprotocol Label Switching (MPLS)
- Quality of Service (QoS)
- Hot Standby Router Protocol (HSRP)

Following are the additional features supported by the 2-Port Gigabit Synchronous Ethernet SPA on the Cisco ASR 1000 Series Aggregation Services Routers:

- L1 clock frequency distribution—In this mode, the 2-Port Gigabit Synchronous Ethernet SPA recovers the received clock, synchronizes it to a traceable source, and uses it to transmit data to the next node.
- A Building Integrated Time Source (BITS) interface for an external Synchronization Supply Unit (SSU) or a BITS device can be used as a clock source, or to clean up the accumulated wander on either a system or a recovered clock.
- The GPS timing interface is used for external GPS devices, and can be selected as either an input or an output reference. The GPS timing interface supports connectivity to the GPS clock.
- In order to maintain a communication channel in synchronous network connections, Ethernet relies on a channel called Ethernet Synchronization Messaging Channel (ESMC) based on the IEEE 802.3 Organization-Specific Slow Protocol. ESMC relays the SSM code that represents the quality level of the Ethernet Equipment Clock (EEC) in a physical layer.
- Supports IP Subscriber Awareness over Ethernet.

Restrictions

These restrictions apply to the 2-Port Gigabit Synchronous Ethernet SPA introduced in Cisco IOS XE Release 3.2:

- Synchronous SPA features are compatible only with the 2-Port Gigabit Synchronous Ethernet SPA.

- The maximum theoretical bandwidth of the 2-Port Gigabit Synchronous Ethernet SPA is 2 Gbps full duplex. The actual performance is limited by the capability of either the host or the jacket card.
- In a failover scenario, the SPA does not perform any auto switchover to a secondary clock source, even if the secondary reference is configured on the same SPA. If the primary clock goes down, the platform explicitly sets the secondary clock as source.
- The Cisco ASR 1002-X Router was introduced in Release 3.7.0S. This router does not support the 2-Port Gigabit Synchronous Ethernet SPA.

These restrictions apply to the 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA introduced in Cisco IOS XE Release 3.3.0S:

- If an Ethernet WAN interface is used as a path terminating equipment (PTE) at one end of a SONET network, only an Ethernet WAN interface can be used for the PTE at the other end of the SONET network. WAN-PHY SPA will neither interoperate nor terminate on either the packet-over-sonet (PoS) or the ethernet-over-sonet (EoS) port at the other end.
- In theory, a 10GBASE-W interface is not intended to interoperate directly with SONET or SDH equipment because WAN-PHY is not fully compliant with SONET or SDH optical and electrical specifications.
- For LAN-PHY, the maximum data rate is 10.3125 gigabit per second (Gbps).
- For WAN-PHY, the maximum data rate is 9.953 gigabit per second (Gbps) (as required by SONET or SDH).

Note The Ethernet hardware used for the Cisco Gigabit Ethernet SPA, including the fixed Gigabit Ethernet ports on the ASR 1000 Series Aggregation Services Routers, can guarantee traffic only at a minimum of 10 bytes Inter-Frame Gap (IFG). If the traffic received is less than 10 bytes IFG, small packet loss can occur. Under certain conditions, some optical transport gear may transmit packets with 8 bytes IFG.

We recommend to set the link mode to transparent mode on the transport gear, as a work around for the problem. Another option is to place an intermediate device such as a L2 switch or media transceiver that can handle the smaller IFG, in between the ASR 1000 Gigabit Ethernet SPA interface and the transport gear.

Prerequisites for Configuring 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA

The prerequisites for configuring 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA are as follows:

- The minimum Cisco IOS XE Software release image required for 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA is Cisco IOS XE Release 3.3.0S or later.
- If the 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA is on LAN or WAN mode at one end, it must run on the same mode (LAN or WAN) at the remote end as well. However, SPA-1X10GE-WL-V2 (configured in LAN mode) is compatible with the SPA-1X10GE-L-V2 (LAN SPA).

Synchronous Ethernet

Synchronous Ethernet (SyncE) is a procedure in which a physical layer interface is used to pass timing from node to node in the same way that timing is passed in SONET or SDH. SyncE, defined by ITU-T standards, such as G.8261, G.8262, G.8264, and G.781, leverages the PHY layer of Ethernet to transmit frequency to remote sites. SyncE over Ethernet provides a cost-effective alternative to the networks. For SyncE to work, each network element must, along with the synchronization path, support SyncE.

The 2-Port Gigabit Synchronous Ethernet SPA has a dedicated external interface known as the BITS interface to recover the clock from a SSU. The Cisco ASR 1000 Series Aggregation Services Routers use this clock for SyncE. The BITS interface supports E1 (European SSUs) and T1 (American BITS) framing. Table 9-1 lists the framing modes for the BITS interface on a 2-Port Gigabit Synchronous Ethernet SPA.

Table 9-1 Framing Modes for BITS Interface

BITS or SSU Interface Support Matrix	Framing Modes Supported	SSM or QL support	Tx Port	Rx Port
T1	T1 ESF	Yes	Yes	Yes
T1	T1 SF	No	Yes	Yes
E1	E1 CRC4	Yes	Yes	Yes
E1	E1 FAS	No	Yes	Yes
E1	E1 CAS	No	No	Yes
E1	E1 CAS CRC4	Yes	No	Yes
2048kHz	2048kHz	No	Yes	Yes

You can implement SyncE on the 2-Port Gigabit Synchronous Ethernet SPA, with four different configurations:

- Clock Recovery from SyncE: The system clock is recovered from the SyncE clocking source (Gigabit and Ten gigabit interfaces only). The router uses this clock as the Tx clock for other SyncE interfaces or ATM or CEoP interfaces.
- Clock Recovery from External Interface: The system clock is recovered from a BITS clocking source or a GPS interface.
- Line to External: The system clock received from an Ethernet is forwarded to an external Synchronization Supply Unit (SSU). During a synchronization chain, the received clock may have unacceptable wander and jitter. The router recovers the clock from the SyncE interface, converts it to the format required for the BITS interface, and sends it to an SSU through the BITS port. The SSU cleans the clock and sends it back to the BITS interface. This clock is used as the Tx clock for the SyncE ports.
- System to External: The system clock is used as the Tx clock for an external interface. By default, the system clock is not transmitted on an external interface.

Squelching

Squelching is a process in which, an alarm indication signal (AIS) is sent to the Tx interfaces whenever the clock source goes down. The squelching functionality is implemented in two scenarios:

- Line to external: If the line source goes down, an AIS is transmitted on the external interface to the SSU.
- System to external: If the router loses all the clock sources, an AIS is transmitted on the external interface to the SSU.

Squelching is performed only on an external device such as an SSU or a Primary Reference Clock (PRC).

SSM and ESMC

Network clocking uses these mechanisms to exchange the quality level of the clock between the network elements:

- Synchronization Status Message
- Ethernet Synchronization Messaging Channel

Synchronization Status Message

Network elements use Synchronization Status Messages (SSM) to inform the neighboring elements about the Quality Level (QL) of the clock. Non-Ethernet interfaces, such as optical interfaces and SONET/T1/E1 SPA framers, use SSM. The key benefits of the SSM are:

- Prevents timing loops.
- Provides quick recovery when a part of the network fails.
- Ensures that a node derives timing from the most reliable clock source.

Ethernet Synchronization Messaging Channel

In order to maintain a logical communication channel in synchronous network connections, Ethernet relies on a channel called Ethernet Synchronization Messaging Channel (ESMC) based on IEEE 802.3 Organization-Specific Slow Protocol standards. ESMC relays the SSM code that represents the quality level of the Ethernet Equipment Clock (EEC) in a physical layer.

The ESMC packets are received only for those ports configured as clock sources, and transmitted on all the SyncE interfaces in the system. These packets are then processed by the clock selection algorithm on RP. and are used to select the best clock. The Tx frame is generated based on the QL value of the selected clock source, and sent to all the enabled SyncE ports.

Clock Selection Algorithm

The clock selection algorithm selects the best available synchronization source from the nominated sources. The algorithm has a non-revertive behavior among clock sources with the same QL value, and always selects the signal with the best QL value. For clock option 1, the default is revertive, and for clock option 2, the default is nonrevertive.

The clock selection process works in the QL-enabled and QL-disabled modes. When multiple selection processes are present in a network element, all processes work in the same mode.

QL-Enabled Mode

In QL-enabled mode, the following parameters contribute to the selection process:

- Quality level
- Signal fail via QL-FAILED

- Priority
- External commands.

Note If no external commands are active, the algorithm selects the reference (for clock selection) with the highest quality level that does not experience a signal fail condition. If multiple inputs have the same highest quality level, the input with the highest priority is selected. For multiple inputs having the same highest priority and quality level, the existing reference is maintained (if it belongs to this group), otherwise an arbitrary reference from this group is selected.

QL-Disabled Mode

In QL-Disabled mode, the following parameters contribute to the selection process:

- Signal failure
- Priority
- IP Subscriber Awareness over Ethernet
- External commands

Note If no external commands are active, the algorithm selects the reference (for clock selection) with the highest priority that does not experience a signal fail condition. For multiple inputs having the same highest priority, the existing reference is maintained (if it belongs to this group). Otherwise an arbitrary reference from this group is selected.

Supported MIBs

The following MIBs are supported by the LAN/WAN Phy Gigabit Ethernet SPAs on the Cisco ASR 1000 Series Aggregation Services Routers:

- ENTITY-MIB
- CISCO-ENTITY-SENSOR-MIB
- ENTITY-SENSOR-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-ALARM-MIB
- IF-MIB
- CISCO-IF-EXTENSION-MIB
- ETHERLIKE-MIB
- CISCO-ETHERLIKE-EXT-MIB
- ETHER-WIS MIB (RFC 3637)
- CISCO-ENTITY-PERFORMANCE-MIB
- CISCO-CLASS-BASED-QOS-MIB
- ENTITY-STATE-MIB
- CISCO-ENTITY-VENDORTYPE-OID-MIB

To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL:

http://tools.cisco.com/ITDIT/MIBS/servlet/index

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml

To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to cco-locksmith@cisco.com. An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

https://tools.cisco.com/RPF/register/register.do

Supported Ethernet SPAs

This section lists and describes the Ethernet SPAs supported by the Cisco ASR 1000 Series Aggregation Services Routers and the SIP line cards supporting these Ethernet SPAs.

2-Port Gigabit Synchronous Ethernet SPA

The 2-Port Gigabit Synchronous Ethernet SPA provides time and frequency distribution across Ethernet networks. Synchronization is not traditionally present in the all-packet networks. Synchronization is cost-effective, and especially important to service providers who have migrated late to packet networks, and use an external time-division multiplexing (TDM) circuit to provide timing to remote networks. These remote networks constantly require synchronization for crucial voice services.

SPA-2X1GE-SYNCE can also interface with either an external SSU or BITS interface or a GPS timing interface. The 2-Port Gigabit Synchronous Ethernet SPA comprises these clock interfaces:

- BITS In
- BITS Out
- GPS In
- GPS Out

The 2-Port Gigabit Synchronous Ethernet SPA (SPA-2X1GE-SYNCE) is compatible with the 2-Port GigE SPA-v2, and provides additional services, such as clock frequency and time-of-day synchronization, using the following technologies:

- Synchronous Ethernet (SyncE)
- ESMC

SyncE defined by ITU-T standards, such as G.8261, G.8262, G.8264, and G.781,and leverages the PHY layer of Ethernet to transmit frequency to remote sites. SyncE provides a cost-effective alternative to the SONET networks. For SyncE to work, each network element must along with the synchronization path, support SyncE.

SPA Architecture

This section provides an overview of the architecture of the Gigabit Ethernet SPAs and describes the path of a packet in the ingress and egress directions. Some of these areas of the architecture are referenced in the SPA software and can be helpful to understand when troubleshooting or interpreting some of the SPA CLI and **show** command output.

Every incoming and outgoing packet on the Gigabit Ethernet SPAs goes through the physical (PHY) SFP optics, the Media Access Controller (MAC), and a Layer 2 Filtering/Accounting ASIC.

Path of a Packet in the Ingress Direction

The following steps describe the path of an ingress packet through the Gigabit Ethernet SPAs:

1. For one-Gigabit Ethernet SPAs, the SFP optics receive incoming frames on a per-port basis from one of the optical fiber interface connectors.
2. For ten-Gigabit Ethernet SPAs, the XFP PHY device processes the frame and sends it over a serial interface to the MAC device.
3. The MAC device receives the frame, strips the CRCs, and sends the packet via the SPI 4.2 bus to the ASIC.
4. The ASIC takes the packet from the MAC devices and classifies the Ethernet information. CAM lookups based on Ethertype, port, VLAN, and source and destination address information determine whether the packet is dropped or forwarded to the SPA interface.

Path of a Packet in the Egress Direction

The following steps describe the path of an egress packet from the SIP through the Gigabit Ethernet SPAs:

1. The packet is sent to the ASIC using the SPI 4.2 bus. The packets are received with Layer 2 and Layer 3 headers in addition to the packet data.
2. The ASIC uses port number, destination MAC address, destination address type, and VLAN ID to perform parallel CAM lookups. If the packet is forwarded, it is forwarded via the SPI 4.2 bus to the MAC device.
3. For Gigabit Ethernet SPAs, the MAC device forwards the packets to the PHY laser-optic interface, which transmits the packet.

Displaying the SPA Hardware Type

To verify the SPA hardware type that is installed in your Cisco ASR 1000 Series Aggregation Services Routers, you can use the **show platform** command.

Table 9-2 shows the hardware description that appears in the **show interfaces** command output for each Gigabit Ethernet SPA that is supported on the Cisco ASR 1000 Series Aggregation Services Routers.

Table 9-2 SPA Hardware Descriptions in show Commands

SPA	Description in show interfaces Command
4-Port Fast Ethernet SPA	Hardware is SPA-4X1FE-TX-V2
8-Port Fast Ethernet SPA	Hardware is SPA-8X1FE-TX-V2
10-Port Gigabit Ethernet SPA	Hardware is SPA-10X1GE-V2
8-Port Gigabit Ethernet SPA	Hardware is SPA-8X1GE-v2
5-Port Gigabit Ethernet SPA	Hardware is SPA-5X1GE-V2
2-Port Gigabit Ethernet SPA	Hardware is SPA-2X1GE-V2
1-Port 10-Gigabit Ethernet SPA	Hardware is SPA-1X10GE-L-V2
1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA	Hardware is SPA-1X10GE-WL-V2.

Note Effective from Cisco IOS XE Release 3.8.0S, support for the Minimal Disruptive Restartfeature is added to the line cards that use the SPA-2X1GE-V2, SPA-5X1GE-V2, SPA-8X1GE-V2, SPA-10X1GE-V2, and SPA-1X10GE-L-V2 Gigabit Ethernet SPAs. For more information on the Minimal Disruptive Restartfeature, see the chapter “Software Upgrade Process” of the *Cisco ASR 1000 Series Aggregation Services Routers Software Configuration Guide*.

Example of the show interfaces Command

The following example shows an output of the **show interfaces tengigabitethernet** command on a Cisco ASR 1000 Series Aggregation Services Routers with a 1-Port 10-Gigabit Ethernet SPA installed in slot 7:

```
Router# show interfaces tengigabitethernet7/0/0
  TenGigabitEthernet0/0/0 is up, line protocol is up (connected)
  Hardware is SPA-1X10GE-L-V2, address is 0000.0c00.0102 (bia 000f.342f.c340)
  Internet address is 15.1.1.2/24
  MTU 1500 bytes, BW 10000000 Kbit, DLY 10 usec,
     reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation ARPA, loopback not set
  Keepalive not supported
  Full-duplex, 10Gb/s
  input flow-control is on, output flow-control is on
  ARP type: ARPA, ARP Timeout 04:00:00
  Last input never, output 00:00:10, output hang never
  Last clearing of "show interface" counters 20:24:30
  Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
  Queueing strategy: fifo
  Output queue: 0/40 (size/max)
  5 minute input rate 0 bits/sec, 0 packets/sec
  5 minute output rate 0 bits/sec, 0 packets/sec
```

```
  L2 Switched: ucast: 0 pkt, 0 bytes - mcast: 0 pkt, 0 bytes
  L3 in Switched: ucast: 0 pkt, 0 bytes - mcast: 0 pkt, 0 bytes mcast
  L3 out Switched: ucast: 0 pkt, 0 bytes mcast: 0 pkt, 0 bytes
     237450882 packets input, 15340005588 bytes, 0 no buffer
     Received 25 broadcasts (0 IP multicasts)
     0 runts, 0 giants, 0 throttles
     0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored
     0 watchdog, 0 multicast, 0 pause input
     0 input packets with dribble condition detected
     1676 packets output, 198290 bytes, 0 underruns
0 output errors, 0 collisions, 4 interface resets
     0 babbles, 0 late collision, 0 deferred
     0 lost carrier, 0 no carrier, 0 PAUSE output
     0 output buffer failures, 0 output buffers swapped out
```

The following example shows a sample output of the **show interfaces gigabitethernet** command on a Cisco ASR 1000 Series Aggregation Services Routers with a 2-Port Gigabit Synchronous Ethernet SPA installed in slot 2:

```
Router# show interfaces gigabitethernet 2/0/1
GigabitEthernet2/0/1 is down, line protocol is down
    Hardware is GigEther SPA, address is 000a.f330.2e40 (bia 000a.f330.2e40)
    Internet address is 2.2.2.1/24
    MTU 1500 bytes, BW 1000000 Kbit, DLY 10 usec,
        reliability 255/255, txload 1/255, rxload 1/255
    Encapsulation ARPA, loopback not set
    Full-duplex, 1000Mb/s, link type is force-up, media type is SX
    output flow-control is on, input flow-control is on
    ARP type: ARPA, ARP Timeout 04:00:00
    Last input 03:19:34, output 03:19:29, output hang never
    Last clearing of "show interface" counters never
    Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
    Queueing strategy: fifo
    Output queue: 0/40 (size/max)
    5 minute input rate 0 bits/sec, 0 packets/sec
    5 minute output rate 0 bits/sec, 0 packets/sec
        1703 packets input, 638959 bytes, 0 no buffer
        Received 23 broadcasts (0 IP multicasts)
        0 runts, 0 giants, 0 throttles
        0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored
        0 watchdog, 1670 multicast, 0 pause input
        1715 packets output, 656528 bytes, 0 underruns
        0 output errors, 0 collisions, 4 interface resets
        0 babbles, 0 late collision, 0 deferred
        0 lost carrier, 0 no carrier, 0 PAUSE output
0 output buffer failures, 0 output buffers swapped out
```

The following example shows a sample output of the **show platform** command on a Cisco ASR 1000 Series Aggregation Services Routers with a 1-Port 10-Gigabit Ethernet LAN/WAN PHY SPA installed in subslots 1,2, and 3 of SIP-40 installed in slot 2:

```
Router# show platform
Chassis type: ASR1013

Slot      Type                State                 Insert time (ago)
--------- ------------------- --------------------- -----------------
2         ASR1000-SIP40       ok                    00:03:08
 2/1      SPA-1X10GE-WL-V2    ok                    00:02:07
 2/2      SPA-1X10GE-WL-V2    ok                    00:02:03
 2/3      SPA-1X10GE-WL-V2    ok                    00:01:59
4         ASR1000-SIP10       ok                    00:03:08
 4/2      SPA-1X10GE-L-V2     ok                    00:02:07
```

```
R0         ASR1000-RP2          ok, active            00:03:08
R1         ASR1000-RP2          ok, standby           00:03:08
F0         ASR1000-ESP40        ok, active            00:03:08
F1         ASR1000-ESP40        ok, standby           00:03:08
P0         ASR1013-PWR-AC       ok                    00:02:19
P1         ASR1013-PWR-AC       ok                    00:02:19
P2         ASR1013-PWR-AC       ok                    00:02:19
P3         ASR1013-PWR-AC       ok                    00:02:18

Slot       CPLD Version         Firmware Version
---------- -------------------- ---------------------------------------
2          00200800             12.2(20090723:220530) [sxiao-cc40g-r...
4          09111601             12.2(33r)XND
R0         10021901             12.2(33r)XND
R1         10021901             12.2(33r)XND
F0         1003190E             15.0(1r)S
F1         1003190E             15.0(1r)S
```

Overview of LAN/WAN-PHY Controllers

LAN/WAN-PHY support in Cisco IOS XE Software Release 3.3.0S and later is based on the IEEE 802.3ae standard. WAN-PHY controllers can only be used as Path Terminating Equipment (PTE). When deploying Ethernet WAN interfaces as endpoints or as PTE between routers, the other endpoint must be an Ethernet WAN interface. WAN-PHY does not interoperate nor terminate on a Packet over Sonet (PoS) or an Ethernet over Sonet (EoS) port.

The purpose of WAN-PHY is to render a 10-Gigabit Ethernet compatible with the SONET STS-192c format and data rate, as defined by ANSI, as well as the SDH VC-4-64c container specified by ITU. To achieve this compatibility, a WAN Interface Sublayer (WIS) is inserted between the 10-Gigabit Ethernet Physical Coding Sublayer (PCS) and the serial Physical Medium Attachment sublayer/Physical Medium Dependent sublayer (PMA/PMD). When the controller is in WAN-PHY mode, the WIS sublayer transports 10-Gigabit Ethernet frames in an OC-192c SONET payload that can interoperate with SONET section or line-level repeaters. This effectively bridges the asynchronous world of Ethernet data with synchronous SONET/SDH transport, allowing the 10-Gigabit Ethernet to be transparently carried over current DWDM networks without having to directly map the Ethernet frames into SONET/SDH.

Following is a list of the WIS characteristics and the functions it performs:

- The WIS allows WAN-PHY equipment to generate an Ethernet data stream to be mapped to an OC-192c or VC-4-64c concatenated payload at the PHY level without any MAC or higher layer processing.
- A 10GBASE-W interface cannot interoperate directly with SONET or SDH equipment because WAN-PHY is not fully compliant with SONET or SDH optical and electrical specifications. In practice, SONET or SDH and 10GBASE-W interfaces can interoperate.
- From a MAC perspective, WAN-PHY does not appear any different from LAN-PHY (no WIS) with the exception of the sustained data rate. In the case of LAN-PHY, the maximum data rate is 10.3125 Gbps, while at WAN-PHY, it is 9.95328 Gbps (as required by SONET or SDH).
- The WIS implements a subset of the SONET functions, including creating the section, line, path overhead headers, calculating the Bit Interleaved Parity (BIP) bytes for error monitoring and managing a variety of alarms and defect indications.

Difference Between POS and 10GBASE-W

- POS and 10GBASE-W cannot interoperate on the same link because the protocol architecture is completely different. POS is based on a serial protocol, such as PPP, whose frames are logically and physically different from the Ethernet MAC frames.
- From a service provider point of view, POS is an L3 point-to-point service, while WAN-PHY is an L2 Ethernet hand-off. It is appropriate to compare WAN-PHY with an Ethernet over SONET (EoS) encapsulation technology, such as ITU-T X.86 or GFP (ITU-T G.7041), where the Ethernet frame is encapsulated in an HDLC-like or GFP frame respectively.
- POS is optically and electrically compatible with SONET and SDH protocols, but WAN-PHY is not.
- POS supports linear Automatic Protection Switching (APS) to restore link failures in 50 ms, while WAN-PHY does not support APS.
- The synchronous nature of POS requires clocking to be configured as either internal or line (Internal clocking is used when the POS interface is connected to another POS back-to-back or through DWDM, while line clocking is required when the POS is connected to a SONET or SDH add/drop multiplexer). WAH-PHY does not support clocking functionality.